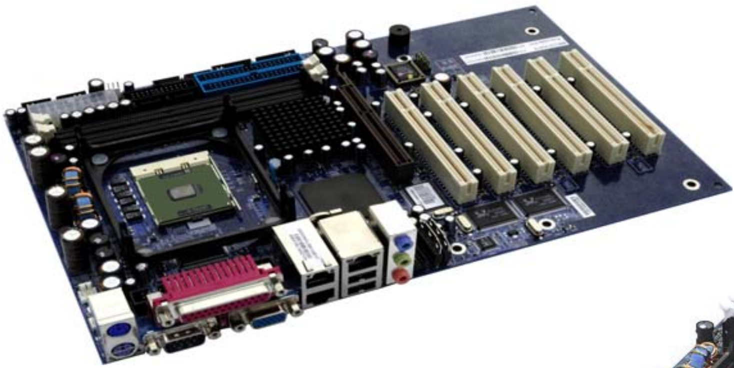
User Manual

for the Mother Boards:

886LCD-M/ATX



886LCD-M/Flex



886LCD-M/mITX



886LCD-M/mITX BGA



Document revision history.

Revision	Date	By	Comment
U	June 22nd 2010	MLA	Minor BIOS information corrections
T	Oct. 13th 2009	MLA	Correction to LAN connector pinning. Battery alternative added. Added "mounting the board to chassis".
S	Nov. 26th 2008	MLA	Added to BIOS: PWM, IRQ5, IRQ7, "Any Harddrive" F11BBS popup control and more info to Security.
R	Aug. 18th 2008	MLA	Arrow for COM3 position on mITX corrected. CPU list updated. Added picture of 886LCD-M/mITX BGA.
Q	May 30th 2008	MLA	Note on Processor Speed displayed in BIOS. Battery type updated.
P	April 22nd 2008	MLA	Battery load information added.
O	Oct. 18th, 2007	MLA	RJ45 pin 4-5 name correction. Note on CDROM audio connector and on ETHER2/3 connector. Corrected text "RTL8100C" to "RTL8110SB-32 in chapter 6.1. Included warning in Installation procedure.
N	Sept. 17th, 2007	MLA	RJ45 pin 4-5 name correction. Note on CDROM audio connector. Removed text RTL8100C from chapter 4.9.2.
M	May 25th, 2007	MLA	ULV 600MHz changed to 800MHz. Suspend LED /HDD LED info added.
L	Mar. 13th, 2007	MLA	Feature port pin 7 text corrected. Chap. 2.1 "Pressing the F2" changed to "Pressing the DEL". ECC not supported.
K	Feb. 16th, 2007	MLA	USB Legacy correction. PS_ON pull-up added. Added more info on BGA CPU.
J	Dec. 13th, 2006	MLA	P_OK pullup removed. CF socket description corrected. Added PCI Riser card info to section "886LCD-M PCI IRQ & INT routing" and to BIOS Riser card setting. Added info to "Onboard Connectors". Size of video memory added to "Component Main Data".
0.1 - J	June 14th, 2004	PJA	*Text removed from rev. U*

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KONTRON Technology's PRODUCTS ARE NOT FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT EXPRESS WRITTEN APPROVAL OF THE GENERAL MANAGER OF KONTRON Technology A/S.

As used herein:
1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

KONTRON Technology Technical Support and Services

If you have questions about installing or using your KONTRON Technology Product, check this User's Manual first – you will find answers to most questions here. To obtain support, please contact your local Distributor or Field Application Engineer (FAE).

Before Contacting Support: Please be prepared to provide as much information as possible:
- CPU Board
  1. Type.
  2. Part-number (Number starting with "53").
  3. Serial Number.
- Configuration
  1. CPU Type, Clock speed.
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup in the Kontron Section).
  4. BIOS Settings different than *Default* Settings (Refer to the Software Manual).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-rom, LCD Panels etc.

Table of contents:

1. Introduction

This manual describes the 886LCD-M/Flex, 886LCD-M/ATX and 886LCD-M/mITX boards made by KONTRON Technology A/S. The boards will also be denoted 886LCD family if no differentiation is required.

All boards are to be used with the Intel® Pentium® M & Intel Celeron® M Processors.

Use of this manual implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the 886 Board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in chapter 3 before switching-on the power.

All configuration and setup of the CPU board is either done automatically or by the user in the CMOS setup menus. Except for the CMOS Clear jumper, no jumper configuration is required.

2. Installation procedure

2.1 Installing the board

To get the board running, follow these steps. In some cases the board shipped from KONTRON Technology has CPU, DDR DRAM and Cooler mounted. In this case Step 2-4 can be skipped.

1. Turn off the PSU (power supply unit).

> ! **Warning**: Do not use Power Supply without 3.3V monitoring watchdog, which is standard feature in ATX Power Supplies.
> Running the board without 3.3V connected will damage the board after a few minutes.

2. Insert the DIMM DDR 184pin DRAM module(s). Be careful to push it in the slot(s) before locking the tabs. For a list of approved DDR DRAM modules contact your Distributor or FAE (list under preparation). DDR333, DIMM 184pin DRAM modules are supported.

3. Install the processor. The CPU is keyed and will only mount in the CPU socket in one way. Use the handle to open/ close the CPU socket. Intel Pentium M and Celeron M processors (Banias processors) are supported.

4. Use heat paste or adhesive pads between CPU and cooler and connect the Fan electrically to the FAN_PROC connector.

5. Insert all external cables for hard disk, keyboard etc. except for flat panel. Connect monitor in order to change CMOS settings to flat panel support etc. To achieve UDMA-66/100 performance on the IDE interface, 80poled UDMA cables **must** be used. If using the IDE_S2 connector care should be taken in correct orientation. The cables that KONTRON provide do not have a key. There is a risk of damaging the HDD or PCB if the cable is not orientated correctly.

> ! **Note**: If the Audio Amplifiers shall be used to generate up to 3W on one or more of the Audio output channels, then make sure that sufficent airflow is around the Audio Amplifier. The Amplifier has integrated Thermal Protection and will not be damaged even though the airflow is insufficient for normal operation.

6. Connect PSU to the board by the ATXPWR connector and turn on power to the PSU.

7. The PWRBTN_IN must be toggled to start the Power supply; this is done by shorting pins 16 (PWRBTN_IN) and pin 18 (GND) on the FRONTPNL connector (see Connector description). A “normally open” switch can be connected via the FRONTPNL connector.

8. Enter the BIOS setup by pressing the “DEL” key during boot up. Refer to the Software Manual (under preparation) for details on BIOS setup.
   Enter Advanced Menu / CPU Configuration / Intel SpeedStep Tech. and select “Maximum Performance”.

Note: To clear all CMOS settings, including Password protection, move the CMOS_CLR jumper (with or without power) for approximately 1 minute. Alternatively turn off power and remove the battery for 1 minute, but be careful to orientate the battery corretly when reinserted.

9. Mounting the board to chassis

> ! **Warning**: When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the Motherboard on a chassis it is recommended using screws with integrated washer and having diameter of ~7mm.
Note: Do not use washers with teeth, as they can damage the PCB mounting hole and may cause short circuits.

2.2 Requirement according to EN60950

Users of 886LCD boards should take care when designing chassis interface connectors in order to fulfill the EN60950 standard:

When an interface/connector has a VCC (or other power) pin, which is directly connected to a power plane like the VCC plane:

To protect the external power lines of peripheral devices the customer has to take care about:

- That the wires have the right diameter to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Lithium Battery precautions:

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3. System specification

3.1 Component main data

The table below summarises the features of the 886LCD-M/Flex, 886LCD-M/ATX and 886LCD-M/mITX embedded motherboards.

Form factor	886LCD-M/Flex: Flex-ATX (190,50mm by 228,60mm) 886LCD-M/ATX: ATX (190,50mm by 304,00mm) 886LCD-M/mITX: mini ITX (170.18mm by 170.18mm)
Processor	• Support for Intel Pentium M and Celeron M Processors in mPGA478 socket with 400MHz system bus. • Banias (0.13um) and Dothan (0.09um) family processors.
Memory	• /Flex and /ATX: 2x184pin DDR SDRAM Dual Inline Memory Module (DIMM) sockets. • /mITX: 1x184pin DDR SDRAM Dual Inline Memory Module (DIMM) socket. • Support for DDR 266/333 (PC2100/PC2700) • Support for 128MB up to 2GB of system memory (/Flex and /ATX) • Support for 128MB up to 1GB of system memory (/mITX) • ECC not supported
Chipset	Intel 855GME Chipset consisting of: • Intel® 855GME Chipset Graphics and Memory Controller Hub (GMCH) • Intel® 6300ESB I/O Controller Hub (ICH) • 4 Mbit Firmware Hub (FWH)
Video	• Intel Extreme Graphics 2 controller • Shared Video Memory up to 32MB/64MB when using min. 128MB/256MB SDRAM. • Analog Display Support, 350-MHz integrated 24-bit RAMDAC with support for analogue monitors up to 2048x1536 at 75 Hz • Digital Video Out Port (DVOB & DVOC) support, dot clock up to 165-MHz DVI DVO ADD and CRT DVO ADD supported. LVDS DVO ADD cards currently not supported • Single or dual channel LVDS panel support (18/ 24bit OpenLDI / SPWG) up to UXGA panel resolution • Dual independent pipe support, Mirror and Dual independent display support Tri-view support through LVDS interface, DVO B/C port, and CRT CRT – LVDS supported CRT - DVO/ Add card supported LVDS - DVO/ Add card supported • AGP 2.0, 1.5V connector (DVO B/C muxed w/ AGP) supporting 1x, 2x, and 4x AGP cards or an AGP Digital Display (ADD) card
Audio	Audio, AC97 version 2.3 subsystem using the Realtek ALC655 codec • Audio Amplifier o /FLEX and /ATX: 4x3W o /mITX: 2x3W • Line-out • CDROM in • SPDIF Interface (Surround) • Microphone Onboard speaker
I/O Control	Winbond W83627THF LPC Bus I/O Controller
Peripheral interfaces	• Four USB 2.0 ports • Four Serial ports (RS232). **Note**: Intel 6300ESB Serial port FIFO (COM C+D) is not standard compliant. May cause issues with specific SW. • One Parallel port, SPP/EPP/ECP / Floppy (optional floppy with special cabling) • Two Serial ATA 150 IDE interfaces, ATA Mode 6 not supported due to Intel Chipset restrictions. • Two Parallel ATA IDE interfaces with UDMA 33, ATA-66/100 support • PS/2 keyboard and mouse ports

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LAN Support	3x 10/100/1000Mbits/s LAN subsystem using Realtek RTL8110SB-32 LAN controllers **or** 1x / 3x 10/100Mbits/s LAN subsystem using Realtek RTL8100C LAN controllers depending on board configuration. PXE and RPL netboot supported. Wake On LAN (WOL) supported (on ETH1 only).
BIOS	• Kontron Technology / AMI BIOS (core version) • Support for Advanced Configuration and Power Interface (ACPI 1.0, 2.0), Plug and Play o Suspend To Ram o Suspend To Disk o Intel Speed Step • Secure CMOS/ OEM Setup Defaults • “Always On” BIOS power setting • RAID Support (RAID modes 0 and 1)
Instantly Available PC Technology	• Support for PCI Local Bus Specification Revision 2.2 • Suspend to RAM support
Expansion Capabilities	• SMBus routed to FEATURE connector • LPC Bus routed to LPC connector • DDC Bus routed to LVDS connector • 8 x GPIOs (General Purpose I/Os) routed to FEATURE connector • PCI Bus routed to PCI slot(s) (PCI Local Bus Specification Revision 2.2)
Hardware Monitor Subsystem	• Smart Fan control system, support Thermal® and Speed® cruise for three onboard Fan control connectors: FAN_PROC, FAN_SYS and FEATURE • Three thermal inputs: CPU die temperature, System temperature and External temperature input routed to FEATURE connector. • Voltage monitoring • Intrusion detect input SMI violations (BIOS) on HW monitor not supported. Supported by API (Windows).
Operating Systems Support	• Win2000 • WinXP • Win98 (USB2.0, ACPI S4 not supported) • Win2003 • WinXP Embedded (limitations may apply) • WinCE.net (limitations may apply) • Linux: Feodora Core 3, Suse 9.2 (limitations may apply)

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Environmental Conditions	**Operating**: 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. 10% - 90% relative humidity (non-condensing) **Storage**: -20°C – 70°C 5% - 95% relative humidity (non-condensing) **Electro Static Discharge (ESD) / Radiated Emissions (EMI):** All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. **Safety:** UL 60950-1:2003, First Edition CSA C22.2 No. 60950-1-03 1st Ed. April 1, 2003 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 **Theoretical MTBF:** 199,799hours (22,8years) , Calculation based on Telcordia SR-332 method. **Restriction of Hazardeous Substances (RoHS):** All boards in the 886LCD-M family is planned for RoHS compliance. **Capacitor utilization:** No Tantal capacitors on board Only Japanese brand Aluminium capacitors rated for 100degrees Celsius used on board
Battery	Exchangeable 3.0V Lithium battery for onboard Real Time Clock and CMOS RAM. Manufacturer Panasonic / PN CR2032NL/LE, CR-2032L/BE or CR-2032L/BN. Approximately 5 years retention varies depending on temperature, actual application on/off rate and variation within chipset and other components. Approximately current draw is 5.3µA (no PSU connected). **CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.**

3.2 Processor support table.

The 886LCD-M/mITX, -/Flex and /ATX are designed to support the following PGA (478 pins) processors:

Intel® Pentium® M Processor, Dothan 90 nm process, FSB 400MHz with 2 MB L2 cache
Intel® Pentium® M Processor, Banias 130 nm process, FSB 400MHz with 1 MB L2 cache
Intel®Celeron® M Processor, Dothan 90 nm process, FSB 400MHz with 1 MB L2 cache
Intel®Celeron® M Processor, Banias 130 nm process, FSB 400MHz with 512 kB L2 cache

Processor Brand	Clock Speed	Processor Number	sSpec no.	Thermal Guideline	Embedded
Intel® Pentium® M, 90nm	2.1 GHz	765	SL7V3	21.0 W	No
	2.0 GHz	755	SL7EM	21.0 W	No
	1.8 GHz	**745**	**SL8U6**	**21.0 W**	**Yes**
	1.8 GHz	**745**	**SL7EN**	**21.0 W**	**Yes**
	1.7 GHz	735	SL7EP	21.0 W	No
	1.6 GHz	725	SL7EG	21.0 W	No
	1.5 GHz	715	SL7GL	21.0 W	No
Intel® Pentium® M, 130nm	1.7 GHz	-	SL6N5	24.5 W	No
	1.6 GHz	**-**	**SL6FA**	**24.5 W**	**Yes**
	1.5 GHz	705	SL6F9	24.5 W	No
	1.4 GHz	-	SL6F8	22.0 W	No
	1.3 GHz	-	SL6N4	22.0 W	No
Intel® Celeron® M, 90nm	**1.5 GHz**	**370**	**SL8MM**	**21.0 W**	**Yes**
	1.5 GHz	**370**	**?**	**21.0 W**	**Yes**
	1.4 GHz	360	SL7LS	21.0 W	No
Intel® Celeron® M, 130nm	1.5 GHz	340	SL7ME	24.5 W	No
	1.3 GHz	**320**	**SL6N7**	**24.5 W**	**Yes**
	1.2 GHz	310	SL6N7	24.5 W	No

The 886LCD-M/mITX(BGA) is a version including an Intel Mobile Celeron ULV 800 MHz BGA CPU (0 L2) an Embedded having TDP (Thermal Design Power) 5.5W (other specifications as for ULV Banias and Dothan).

3.3 System Memory support

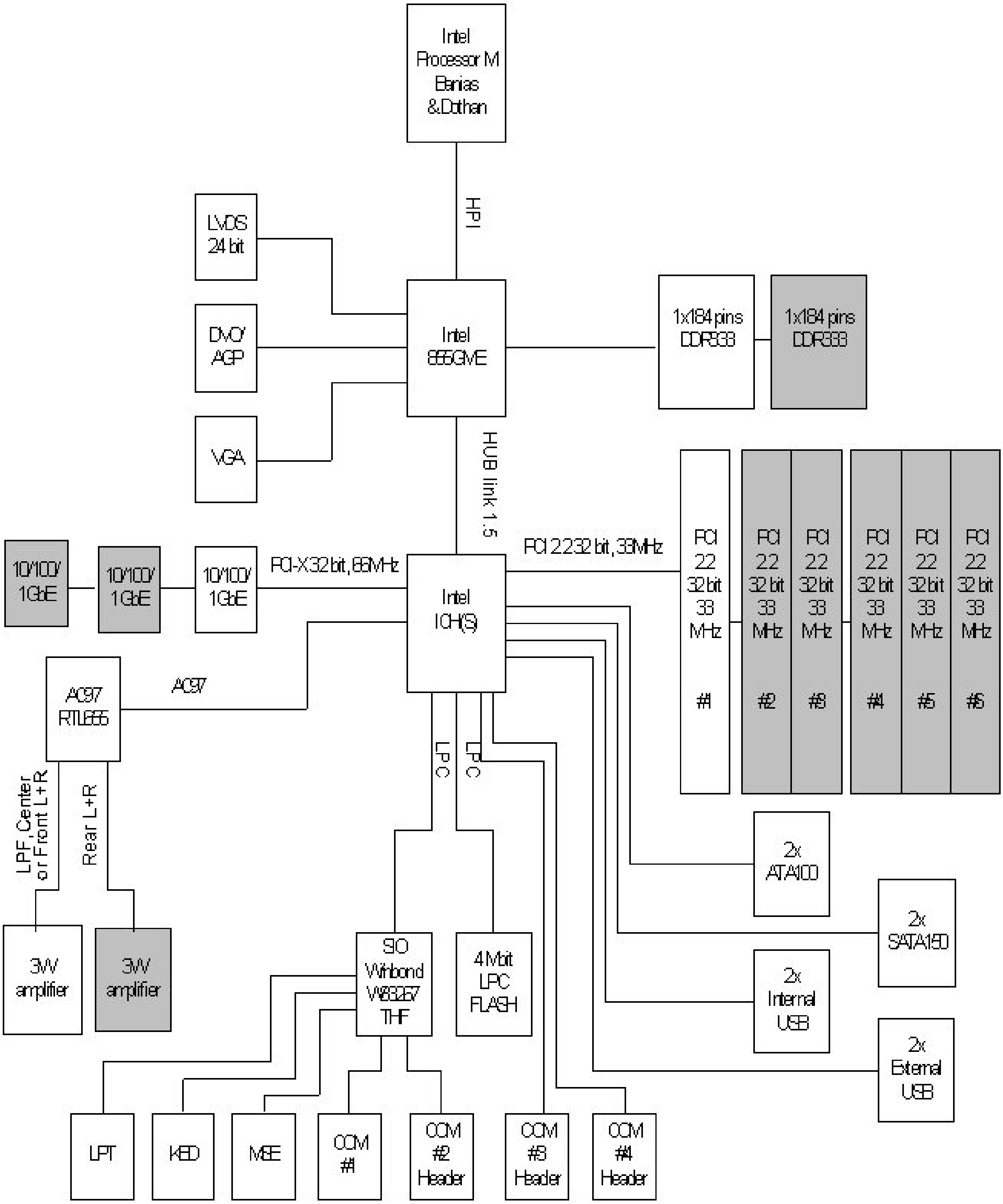
The 886LCD-M/Flex and 886LCD-M/ATX boards have two onboard DIMM sockets (886LCD-M/mITX equipped with one DIMM socket only) and support the following memory features:

- 2.5V (only) 184-pin DDR SDRAM DIMMs with gold-plated contacts
- Supports up to two (one on mITX) single-sided and/or double-sided DIMMs (four rows populated) with unbuffered PC1600/PC2100/PC2700 DDR-SDRAM (without ECC)
- Supports 64 Mbit, 128 Mbit, 256 Mbit and 512 Mbit technologies for x8 and x16 width devices.
- Maximum of 2 Gbytes system (1GB on mITX) memory by using 512 Mbit technology devices (double sided)
- Supports 200 MHz, 266 MHz, and 333 MHz DDR devices
- 64-bit data interface

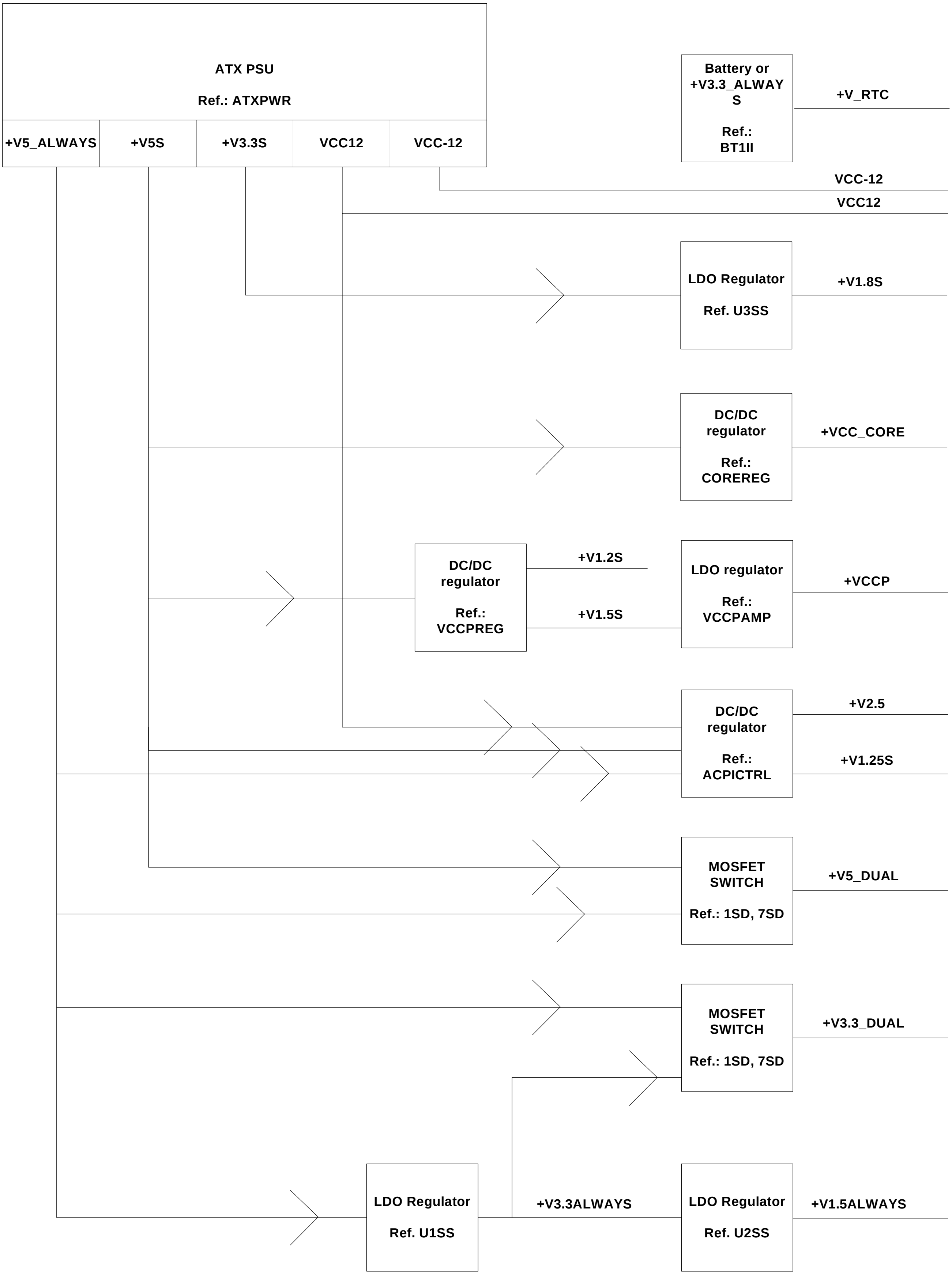
The installed DDR SDRAM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted.

3.4 System overview

The block diagram below shows the architecture and main components of the 886LCD boards. The two key components on the board are the Intel® 855GME and Intel® 6300ESB (ICH(S)) Embedded Chipsets. Components shown shaded are optional depending on board type (886LCD-M/Flex, /ATX or /mITX) and variants of the board.

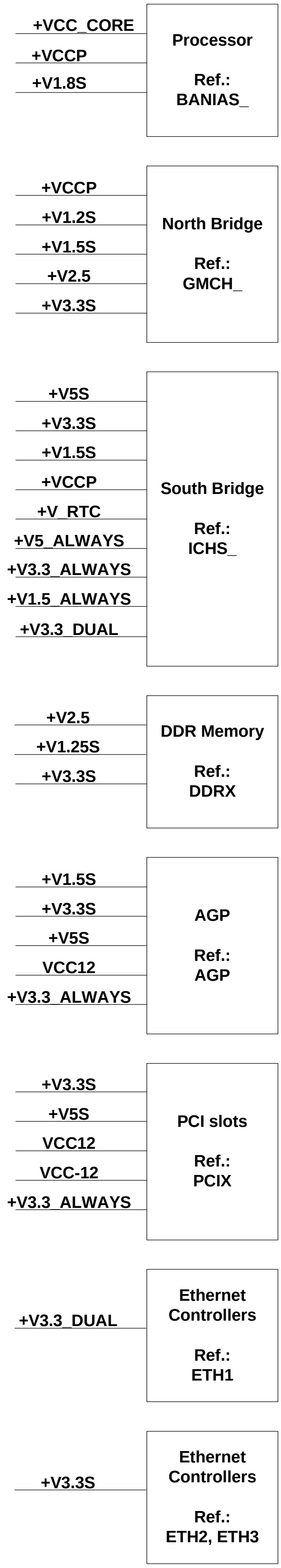


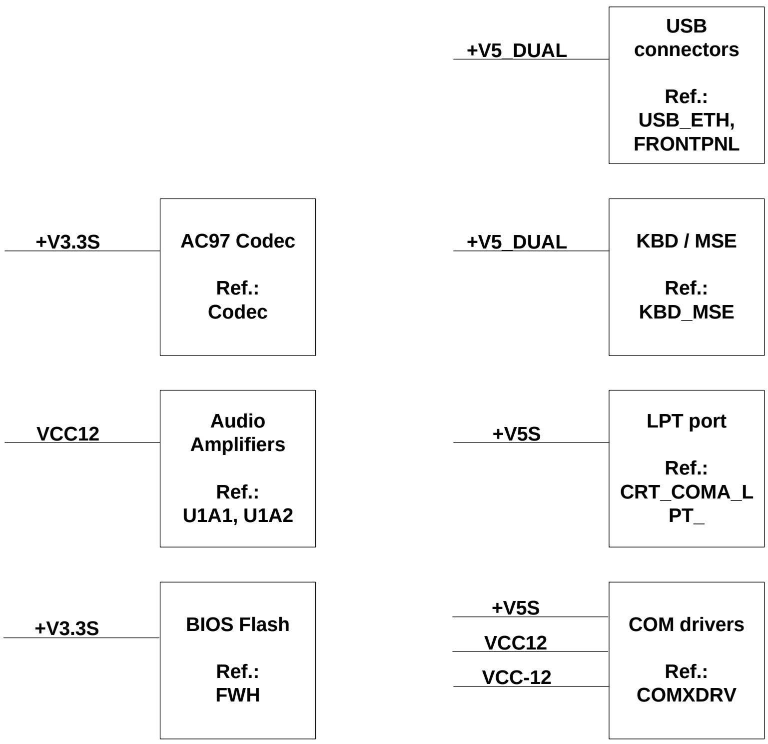
3.5 886LCD-M Power Distribution & Power State Map



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	S0	S3	S5
+V5S	X	N/A	N/A
+V3.3S	X	N/A	N/A
VCC12	X	N/A	N/A
VCC-12	X	N/A	N/A
+V1.8S	X	N/A	N/A
+VCC_CORE	X	N/A	N/A
+VCCP	X	N/A	N/A
+V1.2S	X	N/A	N/A
+V1.5S	X	N/A	N/A
+V2.5	X	X	N/A
+V1.25S	X	N/A	N/A
+V5_DUAL	X	X	N/A
+V3.3_DUAL	X	X	N/A
+V5_ALWAYS	X	X	N/A
+V3.3ALWAYS	X	X	N/A
+V1.5ALWAYS	X	X	N/A
+V_RTC	X	X	X





3.6 Power Consumption

This section lists a summary of the power consumption of the 886LCD-M Boards. For additional details, please refer to the Power Supply Characteristics document available from Kontron Technology.

The idle/full power consumption of the 886LCD-M is measured under:

1- DOS prompt idle/full CPU load.

2- WindowsXP idle/full CPU load.

3.6.1 Test system configuration

The following items were used in the test setup:

1. 886LCD-M/Flex board (710180-4500) with 256MB SDRAM (333MHz) EZ128DDR16M168-333INF.
2. Pentium-M 1600/400Mhz (1MB Cache) CPU.
3. Standard Pentium-4 active CPU cooler.
4. PS/2 keyboard & mouse.
5. CRT.
6. Primary Master HD (Fujitsu MPG3102AT 10.24GB).
7. ATX PSU (Antec 550W)
8. Tektronix TDS 620B, P6243 probes
9. Fluke Current Probe 80i-100S AC/DC
10. Ethernet Ports 1, 2, 3 are enabled (10/100/1000MB LAN).

3.6.2 Measured Power Consumption, Net

886LCD-M board (3x1GB LAN) with: Pentium M 1600/400MHz (1MB L2 Cache), 256MB DDR RAM (333MHz)

Power State	Net	Current (I)	Power (W)
DOS FULL LOAD	+5VDC	4.560A	22.8W
	+3.3VDC	2.568A	8.7W
DOS IDLE	+5VDC	4.028A	20.3W
	+3.3VDC	2.532A	8.6W
	+12VDC	0.424A	4.6W
ACPI S1	+5VDC	1.758A	8.8W
	+3.3VDC	2.560A	8.8W
ACPI S3	+5VSB	1.007A	5.16W
ACPI S4	+5VSB	1.007A	4.95W
ACPI S5	+5VSB	0.892A	4.6W
WINDOWS XP IDLE	+5VDC	2.212A	11.1W
	+3.3VDC	2.720A	8.7W
WINDOWS XP FULL LOAD	+5VDC	4.704A	23.7W
	+3.3VDC	2.572A	8.7W

3.6.3 Power Consumption, Total

886LCD-M board (3x1GB LAN) with Pentium M 1600/400MHz (1MB L2 Cache), 256MB DDR RAM (333MHz)

Power State	CPU Speed	Power consumption
Full load	1600Mhz	37.0W
Idle	1600Mhz	24.4W
ACPI S1	1600Mhz	22.2W
ACPI S3	1600Mhz	5.16W
ACPI S4	1600Mhz	4.95W
ACPI S5	1600Mhz	4.60W

886LCD-M board (3x1GB LAN) with Intel Mobile Celeron 800/400MHz (0MB L2 Cache) BGA, 256MB DDR RAM (333MHz)

Power State	CPU Speed	Power consumption
Full load	800MHz	28.4W
Idle	800MHz	22.8W
ACPI S1	800MHz	21.6W
ACPI S3	800MHz	5.16W
ACPI S4	800MHz	4.95W
ACPI S5	800MHz	4.60W

3.6.4 Minimum recommended power supply specifications

Note: Minimum recommended power supply specifications do not include attachment of AUDIO Speakers (AMP-out), USB, AGP, PCI devices. If these devices are added to the board, additional power requirements must be taken into account. Refer to the "Detailed Device Power consumption" section.

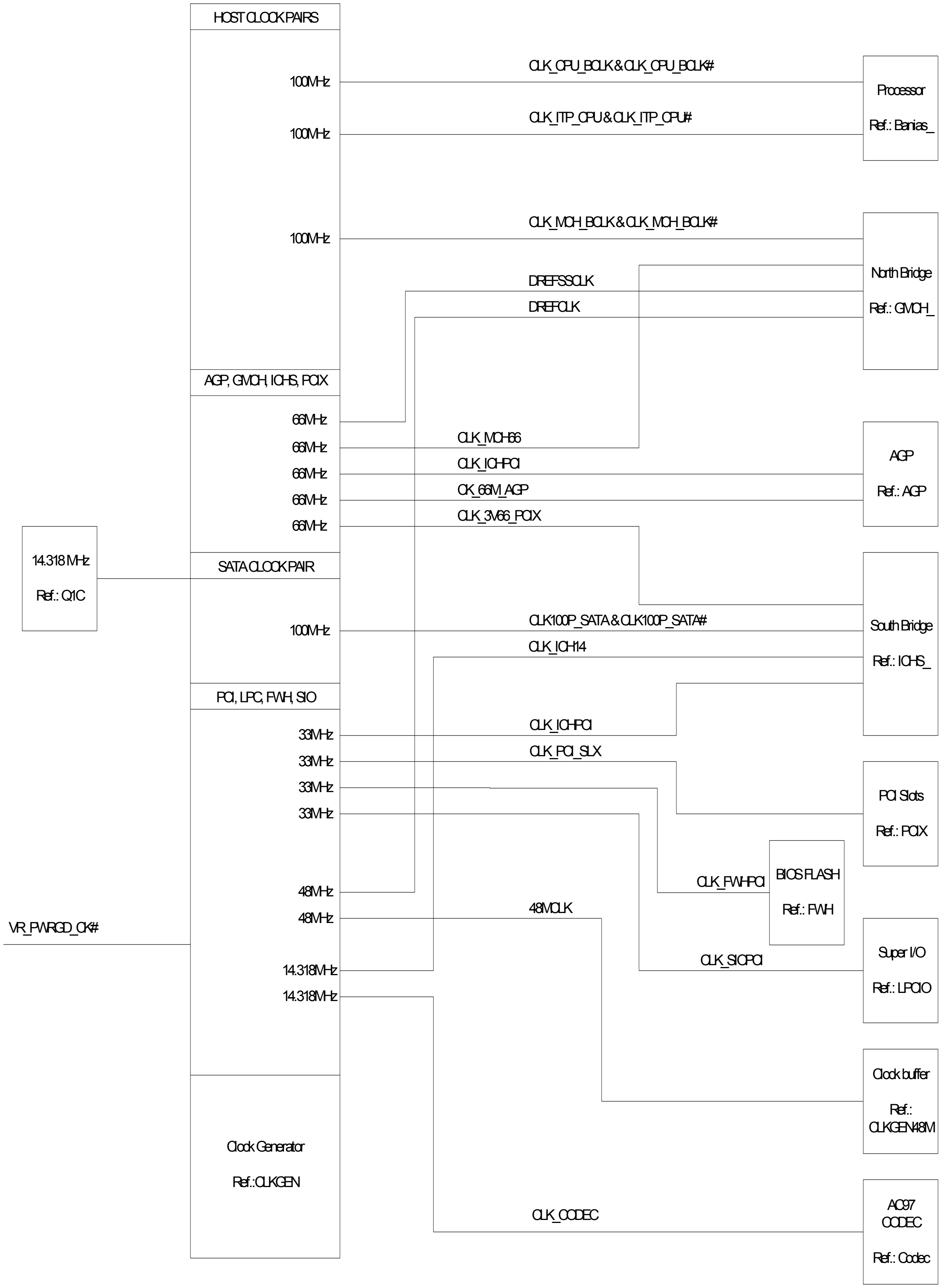
Net	Current (I)	Peak Current
+5VDC	8.0A	40.0A(3ms)
+3.3VDC	4.0A	14.0A(3ms)
+12VDC	0.6A	6.0A(4ms)
+5VSB	1.2A	3.5A(14ms)
-12 VDC	0.2A	1.0A(4ms)
-5VDC	N/A	N/A

3.6.5 Recommended Power Supply specifications

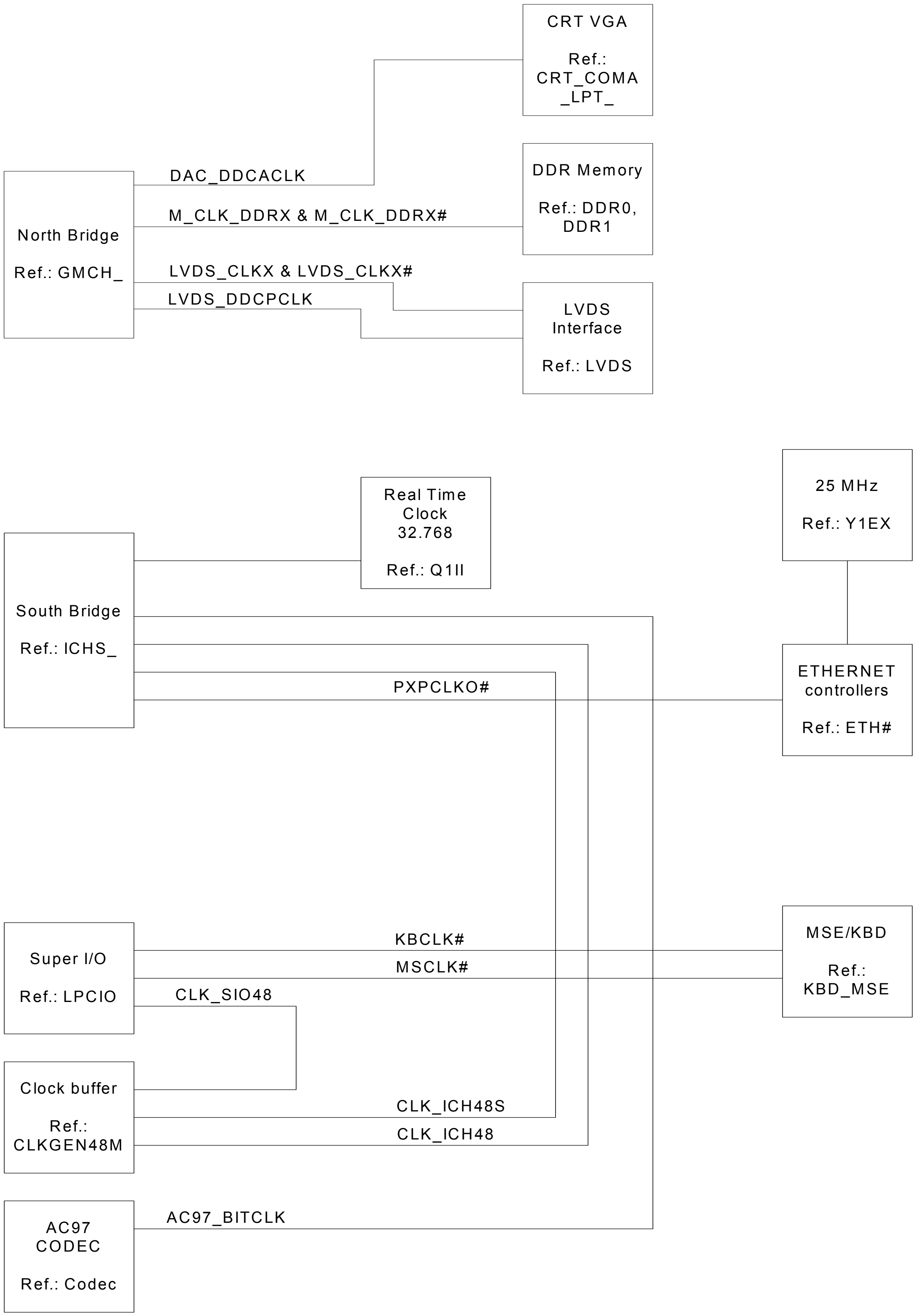
Note: Recommended power supply specifications, includes attachment of COM, Fan, 4xAudio Speakers 4/8ohm, USB, AGP, PCI devices.

Net	Current (I)	Peak Current
+5VDC	18.0A	50.0A(3ms)
+3.3VDC	7.0A	20.0A(3ms)
+12VDC	6.0A	8.0A(4ms)
+5VSB	2.0A	5.0A(14ms)
-12 VDC	0.5A	1.0A(4ms)
-5VDC	N/A	N/A

3.7 886LCD-M Clock Distribution



(continues)


CRT VGA
Ref.: CRT_COMA _LPT_
DDR Memory
Ref.: DDR0, DDR1
North Bridge
Ref.: GMCH_
DAC_DDCACLK
M_CLK_DDRX & M_CLK_DDRX#
LVDS_CLKX & LVDS_CLKX#
LVDS_DDCPCLK
LVDS Interface
Ref.: LVDS
Real Time Clock 32.768
Ref.: Q1II
25 MHz
Ref.: Y1EX
South Bridge
Ref.: ICHS_
PXPCLKO#
ETHERNET controllers
Ref.: ETH#
Super I/O
Ref.: LPCIO
KBCLK#
MSCLK#
CLK_SIO48
MSE/KBD
Ref.: KBD_MSE
Clock buffer
Ref.: CLKGEN48M
CLK_ICH48S
CLK_ICH48
AC97 CODEC
Ref.: Codec
AC97_BITCLK

4. Connector Definitions

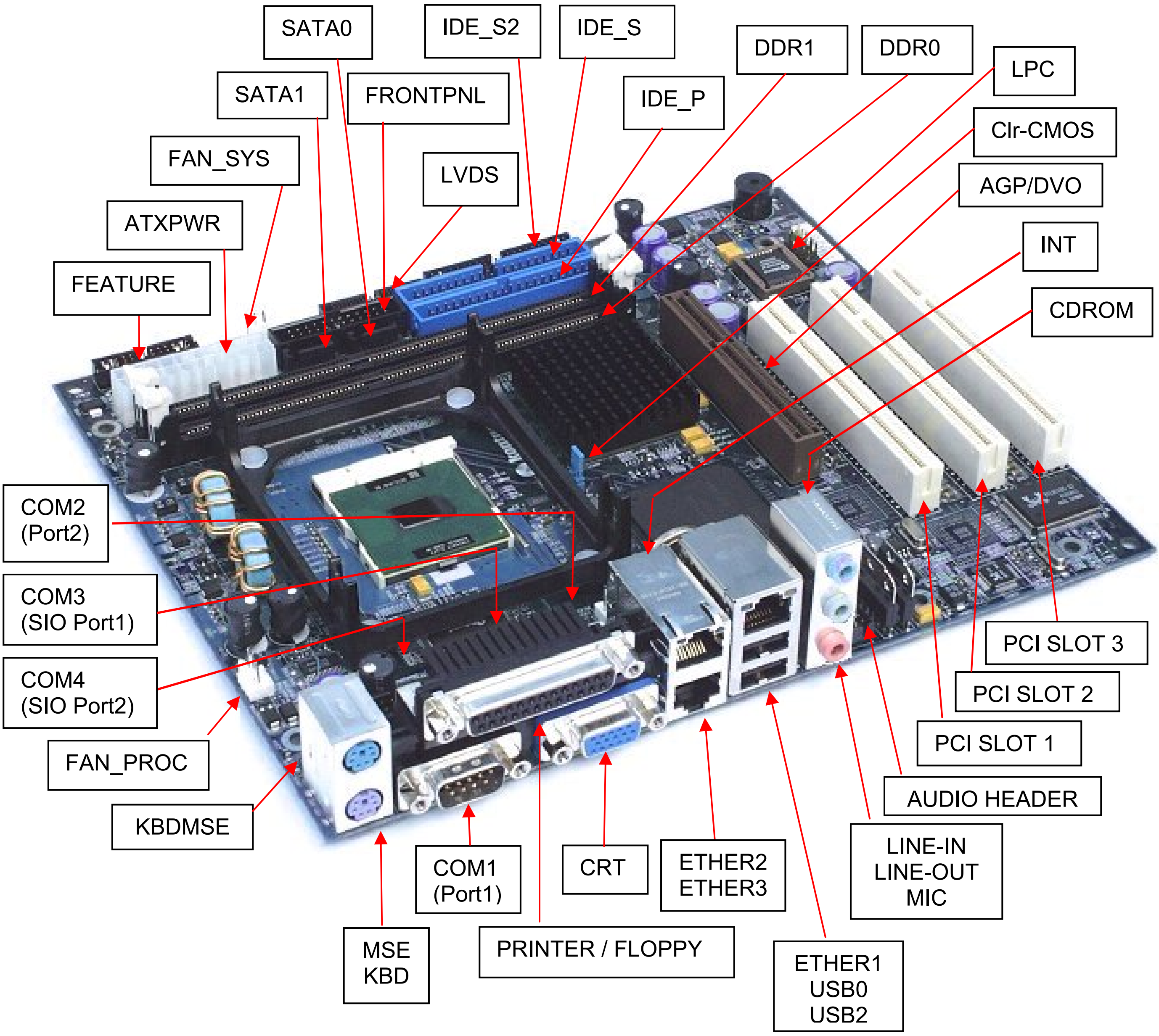
The following sections provide pin definitions and detailed description of all on-board connectors.
.
The connector definitions follow the following notation:

Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation “XX#” states that the signal “XX” is active low.
Type	AI: Analog Input. AO: Analog Output. I: Input, TTL compatible if nothing else stated. IO: Input / Output. TTL compatible if nothing else stated. IOT : Bi-directional tristate IO pin. IS: Schmitt-trigger input, TTL compatible. IOC: Input / open-collector Output, TTL compatible. NC: Pin not connected. O: Output, TTL compatible. OC: Output, open-collector or open-drain, TTL compatible. OT: Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR: Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

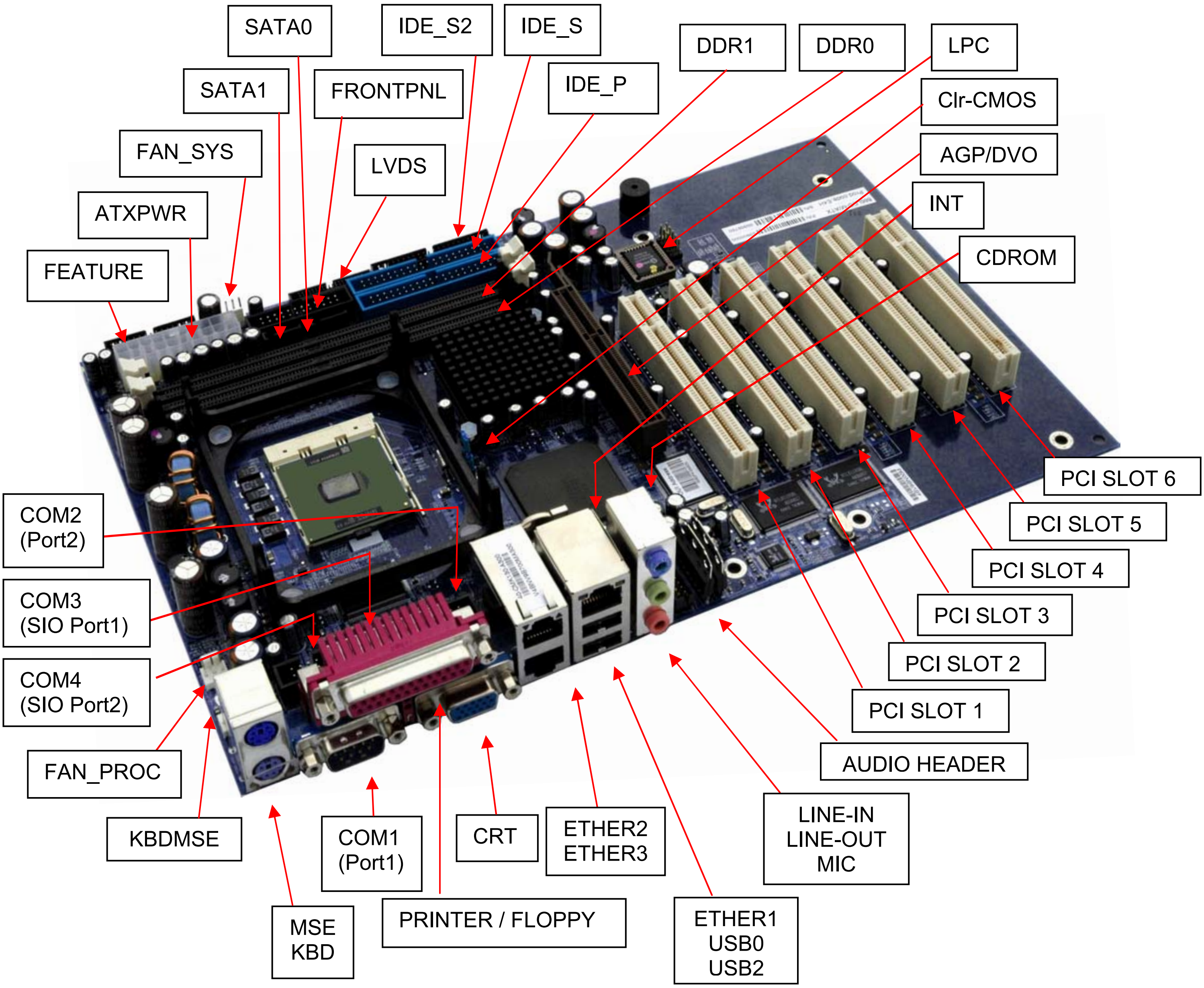
The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

4.1 Connector layout

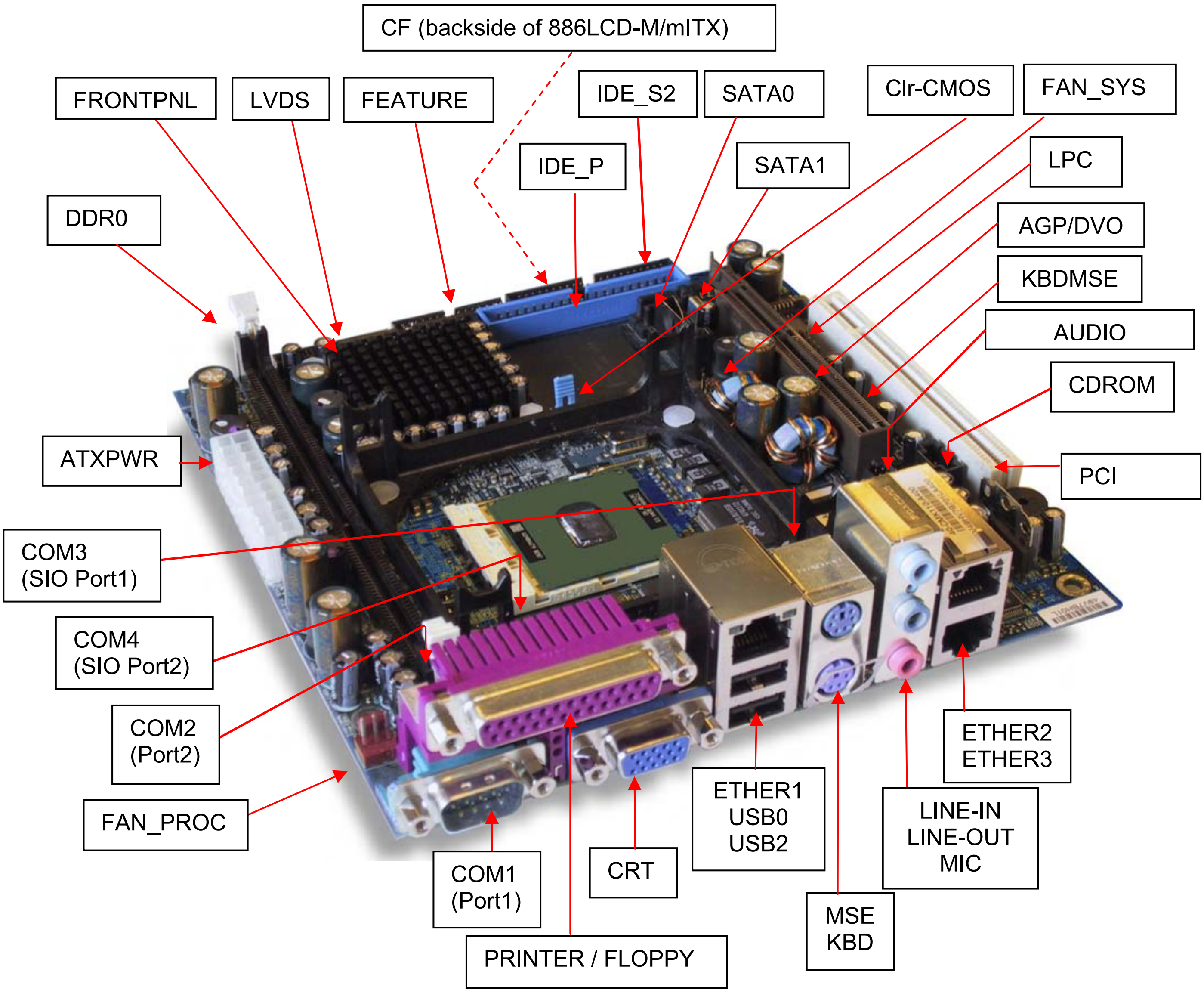
4.1.1 886LCD-M/Flex

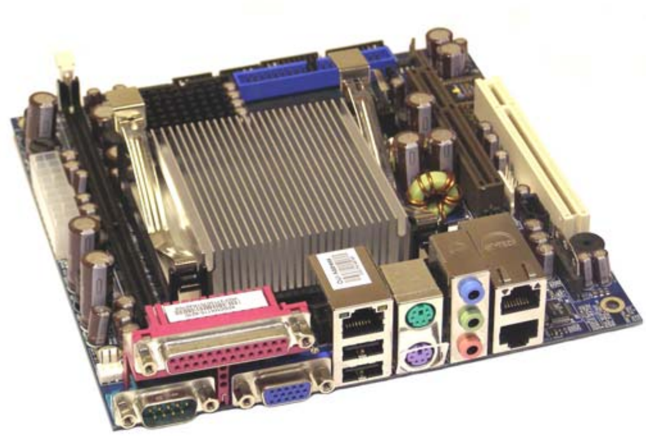


4.1.2 886LCD-M/ATX



4.1.3 886LCD-M/mITX





886LCD-M/mITX BGA

4.2 Power Connector (ATXPWR)

The 886LCD-M/Flex, 886LCD-M/ATX and 886LCD-M/mITX is designed to be supplied from a standard ATX power supply.

Power Connector 886LCD-M/Flex, 886LCD-M/ATX and 886LCD-M/mITX

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	+12V	10	20	5V	PWR	-	-	
	-	-	PWR	SB5V	9	19	5V	PWR	-	-	
2	-	-	I	P_OK	8	18	-5V	PWR	-	-	1
	-	-	PWR	GND	7	17	GND	PWR	-	-	
	-	-	PWR	5V	6	16	GND	PWR	-	-	
	-	-	PWR	GND	5	15	GND	PWR	-	-	
	-	-	PWR	5V	4	14	PSON#	OC	-	22K/	3
	-	-	PWR	GND	3	13	GND	PWR	-	-	
	-	-	PWR	3V3	2	12	-12V	PWR	-	-	
	-	-	PWR	3V3	1	11	3V3	PWR	-	-	

Note 1: -5V supply is not used onboard.
Note 2: 4K7 pull-up resistor on old board revision.
Note 3: Pull-up to +5VSB.

The requirements to the supply voltages are as follows (also refer to ATX specification version 2.03):

Supply	Min	Max	Tolerance
3V3	3.14V	3.46V	+/-5%
5V	4.75V	5.25V	+/-5%
SB5V	4.75V	5.25V	+/-5%
+12V	11.4V	12.6V	+/-5%
–12V	–13.2V	–10.8V	+/-10%

Control signal description:

Signal	Description
P_OK	Active high signal from the power supply indicating that the 5V and 3V3 supplies are within operating limits. It is strongly recommended to use an ATX supply with the 886LCD-M/Flex, 886LCD-M/ATX and 886LCD-M/mITX boards, in order to implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised onboard the 886LCD-M/Flex, 886LCD-M/ATX and 886LCD-M/mITX boards.
PS_ON#	Active low open drain output with pull-up to Standby +5V. Used to turn on power supply outputs.

4.3 Keyboard and PS/2 mouse connectors

Attachment of a keyboard or PS/2 mouse adapter can be done through the stacked PS/2 mouse and keyboard connector (MSE & KBD).

Both interfaces utilize open-drain signaling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from 5V_STB when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resetable fuse.

4.3.1 Stacked MINI-DIN keyboard and mouse Connector (MSE & KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	-	NC	6	5	MSCLK	IOC	TBD	4K7	
	-	-	PWR	5V/SB5V	4	3	GND	PWR	-	-	
	-	-	-	NC	2	1	MSDAT	IOC	TBD	4K7	
			-	NC	6	5	KBDCLK	IOC	TBD	4K7	
	-	-	PWR	5V/SB5V	4	3	GND	PWR	-	-	
	-	-	-	NC	2	1	KBDDAT	IOC	TBD	4K7	

Signal Description – Keyboard & and mouse Connector (MSE & KBD), see below.

4.3.2 keyboard and mouse pin-row Connector (KBDMSE)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOC	TBD	4K7	
2	KBDDAT	IOC	TBD	4K7	
3	MSCLK	IOC	TBD	4K7	
4	MSDAT	IOC	TBD	4K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

4.4 Display Connectors

The 886LCD board family provides onboard two basic types of interfaces to a display: Analog CRT interface and a digital interface typically used with flat panels. The digital interface to flat panels can be achieved through the onboard LVDS dual channel interface and/or the DVO port available on the AGP connector.

4.4.1 CRT Connector (CRT)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN			Signal	Type	Ioh/Iol	Pull U/D	Note
						6		ANA-GND	PWR	-	-	
	/75R	*	A0	RED	1		11	NC	-	-	-	
						7		ANA-GND	PWR	-	-	
	/75R	*	A0	GREEN	2		12	DDCDAT	IO	TBD	2K2	
						8		ANA-GND	PWR	-	-	
	/75R	*	A0	BLUE	3		13	HSYNC	O	TBD		
						9		5V	PWR	-	-	1
	-	-	-	NC	4		14	VSYNC	O	TBD		
						10		DIG-GND	PWR	-	-	
	-	-	PWR	DIG-GND	5		15	DDCCLK	IO	TBD	2K2	

Note 1: The 5V supply in the CRT connector is fused by a 1.1A reset-able fuse.

Signal Description - CRT Connector:

Signal	Description
HSYNC	CRT horizontal synchronization output.
VSYNC	CRT vertical synchronization output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red color signal to the CRT. For 75 Ohm cable impedance.
GREEN	Analog output carrying the green color signal to the CRT. For 75 Ohm cable impedance.
BLUE	Analog output carrying the blue color signal to the CRT. For 75 Ohm cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.

4.4.2 LVDS Flat Panel Connector (LVDS)

Note	Type	Signal	Pin		Signal	Type	Note
Max. 0.5A	PWR	+12V	1	2	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	3	4	+12V	PWR	Max. 0.5A
Max. 0.5A	PWR	+12V	5	6	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	+5V	7	8	GND	PWR	Max. 0.5A
Max. 0.5A	PWR	LCDVCC	9	10	LCDVCC	PWR	Max. 0.5A
4K7Ω, 3.3V	OT	DDC CLK	11	12	DDC DATA	OT	4K7Ω, 3.3V
3.3V level	OT	BKLTCTL	13	14	VDD ENABLE	OT	3.3V level
3.3V level	OT	BKLTEN#	15	16	GND	PWR	Max. 0.5A
	LVDS	LVDS A0-	17	18	LVDS A0+	LVDS	
	LVDS	LVDS A1-	19	20	LVDS A1+	LVDS	
	LVDS	LVDS A2-	21	22	LVDS A2+	LVDS	
	LVDS	LVDS ACLK-	23	24	LVDS ACLK+	LVDS	
	LVDS	LVDS A3-	25	26	LVDS A3+	LVDS	
Max. 0.5A	PWR	GND	27	28	GND	PWR	Max. 0.5A
	LVDS	LVDS B0-	29	30	LVDS B0+	LVDS	
	LVDS	LVDS B1-	31	32	LVDS B1+	LVDS	
	LVDS	LVDS B2-	33	34	LVDS B2+	LVDS	
	LVDS	LVDS BCLK-	35	36	LVDS BCLK+	LVDS	
	LVDS	LVDS B3-	37	38	LVDS B3+	LVDS	
Max. 0.5A	PWR	GND	39	40	GND	PWR	Max. 0.5A

Signal Description – LVDS Flat Panel Connector:

Signal	Description
LVDS A0..A3	LVDS A Channel data
LVDS ACLK	LVDS A Channel clock
LVDS B0..B3	LVDS B Channel data
LVDS BCLK	LVDS B Channel clock
BKLTCTL	Backlight control (1), PWM signal to implement voltage in the range 0-3.3V
BKLTEN#	Backlight Enable signal (active low) (2)
VDD ENABLE	Output Display Enable.
LCDVCC	VCC supply to the flat panel. This supply includes power-on/off sequencing. The flat panel supply may be either 5V DC or 3.3V DC depending on the CMOS configuration. Maximum load is 1A at both voltages.
DDC CLK	DDC Channel Clock
DDC DATA	DDC Channel Data

Note 1) Windows API (version Hwmon_KTAPI ver 4.5 or newer) is available to operate the BKLTCTL signal. Some Inverters has a limited voltage range 0- 2.5V for this signal. If voltage is > 2.5V the Inverter might latch up. Some Inverters generates noise to the BKLTCTL signal and this noise can make the lvds transmision fail resulting in corrupted picture on the display. By adding 1K Ohm resistor in series with this signal and mounted in the Inverter end of the cable kit the noise is limited and picture is stabil.

Note 2) If the Backlight Enable is required to be active high then make the BIOS Chipset setting: Backlight Signal Inversion = Enabled.

4.4.3 AGP/DVO connector

Note	Type	Signal	PIN		Signal	Type	Note
		OVRCNT	B1	A1	+12V	PWR	
	PWR	+5V	B2	A2	TYPEDET		
	PWR	+5V	B3	A3	RSVD		
		USB+	B4	A4	USB-		
	PWR	GND	B5	A5	GND	PWR	
		INTB	B6	A6	INTA		
		AGPCLK	B7	A7	RST-		
		GREQ	B8	A8	GGNT		
	PWR	+3.3V	B9	A9	+3.3V	PWR	
		ST0	B10	A10	ST1		
		ST2	B11	A11	RSVD		
	I	RBF	B12	A12	PIPE	I	
	PWR	GND	B13	A13	GND	PWR	
		RSVD	B14	A14	WBF	I	
	I	ADD_ID0	B15	A15	ADD_ID1	I	
	PWR	+3.3V	B16	A16	+3.3V	PWR	
	I	ADD_ID2	B17	A17	ADD_ID3	I	
	I	ADD_RS	B18	A18	ADD_RS		
	PWR	GND	B19	A19	GND	PWR	
	I	ADD_ID4	B20	A20	ADD_ID5	I	
	I	ADD_ID6	B21	A21	ADD_ID7	I	
		RSVD	B22	A22	RSVD		
	PWR	GND	B23	A23	GND	PWR	
	PWR	3V3AUX	B24	A24	RSVD		
	PWR	+3.3V	B25	A25	+3.3V	PWR	
		DVOC_Fld/Stl	B26	A26	DVOBC_Intr-		
		DVOC_D10	B27	A27	DVOC_D11		
	PWR	+3.3V	B28	A28	+3.3V	PWR	
		DVOC_D8	B29	A29	DVOC_D9		
		DVOC_D6	B30	A30	DVOC_D7		
	PWR	GND	B31	A31	GND	PWR	
		DVOC_Clk+	B32	A32	DVOC_Clk-		
		DVOC_D4	B33	A33	DVOC_D5		
	PWR	+1.5V	B34	A34	+1.5V	PWR	
		DVOC_D2	B35	A35	DVOC_D3		
		DVOC_D0	B36	A36	DVOC_D1		
	PWR	GND	B37	A37	GND	PWR	
		DVOC_Hsync	B38	A38	DVOC_Blank-		
		ADD_RS	B39	A39	DVOC_Vsync		
	PWR	+1.5V	B40	A40	+1.5V	PWR	
		M_I2CClk	B41	A41	M_DVI_Data		
		M_I2CData	B46	A46	M_DVI_Clk		
	PWR	+1.5V	B47	A47	M_DDCData		
		GPERR	B48	A48	PME		
	PWR	GND	B49	A49	GND	PWR	
		GSERR	B50	A50	ADD_Detect		
		DVOB_Blank-	B51	A51	M_DDCClk		
	PWR	+1.5V	B52	A52	+1.5V	PWR	
		DVOB_Fld/Stl	B53	A53	DVOBC_ClkInt		
		DVOB_D10	B54	A54	DVOB_D11		
	PWR	GND	B55	A55	GND	PWR	
		DVOB_D8	B56	A56	DVOB_D9		
		DVOB_D6	B57	A57	DVOB_D7		
	PWR	+1.5V	B58	A58	+1.5V	PWR	
		DVOB_Clk+	B59	A59	DVOB_Clk-		
		DVOB_D4	B60	A60	DVOB_D5		
	PWR	GND	B61	A61	GND	PWR	
		DVOB_D2	B62	A62	DVOB_D3		
		DVOB_D0	B63	A63	DVOB_D1		
	PWR	+1.5V	B64	A64	+1.5V	PWR	
		DVOB-Vsync	B65	A65	DVOB_Hsync		
		VREFCG	B66	A66	VREFGC		

The AGP buffers operate only in 1.5V mode (not 3.3-V tolerant). The AGP interface supports 1x/2x/4x AGP signaling and 2x/4x Fast Writes.

Signal Description – AGP Connector:

Signal	Description
Address	
PIPE#	**Pipelined Read:** This signal is asserted by the AGP master to indicate a full width address is to be enqueued on by the target using the **AD** bus. One address is placed in the AGP request queue on each rising clock edge while **PIPE#** is asserted. When **PIPE#** is deasserted no new requests are queued across the AD bus. **During SBA Operation:** This signal is **not used** if SBA (Side Band Addressing) is selected. **During FRAME# Operation:** This signal is **not used** during AGP FRAME# operation. **PIPE#** is a sustained tri-state signal from masters (graphics controller), and is an input to the GMCH
ADD_ID[7:0]	**Side-band Address:** These signals are used by the AGP master (graphics controller) to pass address and command to the GMCH. The **SBA** bus and AD bus operate independently. That is, transactions can proceed on the **SBA** bus and the AD bus simultaneously. **During PIPE# Operation:** These signals are **not used** during PIPE# operation. **During FRAME# Operation:** These signals are **not used** during AGP FRAME# operation. **NOTE:** When sideband addressing is disabled, these signals are isolated (no external/internal pull-ups are required).
Flow control	
RBF#	**Read Buffer Full:** Read buffer full indicates if the master is ready to accept previously requested low priority read data. When **RBF#** is asserted the GMCH is not allowed to initiate the return low priority read data. That is, the GMCH can finish returning the data for the request currently being serviced. **RBF#** is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.
WBF#	**Write-Buffer Full:** indicates if the master is ready to accept Fast Write data from the GMCH. When **WBF#** is asserted the GMCH is not allowed to drive Fast Write data to the AGP master. **WBF#** is only sampled at the beginning of a cycle. If the AGP master is always ready to accept fast write data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.
AGP Status	
ST[2:0]	**Status:** Provides information from the arbiter to an AGP Master on what it may do. **ST[2:0]** only have meaning to the master when its **GNT#** is asserted. When **GNT#** is deasserted these signals have no meaning and must be ignored. **ST[2:0 Meaning** **000** Previously requested low priority read data is being returned to the master **001** Previously requested high priority read data is being returned to the master **010** The master is to provide low priority write data for a previously queued write command **011** The master is to provide high priority write data for a previously queued write command **100** Reserved **101** Reserved **110** Reserved **111** The master has been given permission to start a bus transaction. The master may queue AGP requests by asserting **PIPE#** or start a PCI transaction by asserting **FRAME#**.
AGP Strobes	
ADSTB[0]	**Address/Data Bus Strobe-0:** provides timing for 2x and 4x data on **AD[15:0]** and **C/BE[1:0]#** signals. The agent that is providing the data will drive this signal.
ADSTB#[0]	**Address/Data Bus Strobe-0 Complement:** With AD STB0, forms a differential strobe pair that provides timing information for the **AD[15:0]** and **C/BE[1:0]#** signals. The agent that is providing the data will drive this signal.
ADSTB[1]	**Address/Data Bus Strobe-1:** Provides timing for 2x and 4x data on **AD[31:16]** and **C/BE[3:2]#** signals. The agent that is providing the data will drive this signal.
ADSTB#[1]	**Address/Data Bus Strobe-1 Complement:** With AD STB1, forms a differential strobe pair that provides timing information for the AD[15:0] and C/BE[1:0]**#** signals in 4X mode. The agent that is providing the data will drive this signal.
SBSTB	**Sideband Strobe:** Provides timing for 2x and 4x data on the **SBA[7:0]** bus. It is driven by the AGP master after the system has been configured for 2x or 4x sideband address mode.
SBSTB#	**Sideband Strobe Complement:** The differential complement to the **SB_STB** signal. It is used to provide timing 4x mode.

(continues)

AGP/PCI Signals-Semantics	
FRAME#	**G_FRAME:** Frame. **During PIPE# and SBA Operation:** Not used by AGP SBA and PIPE# operations. **During Fast Write Operation:** Used to frame transactions as an output during Fast Writes. **During FRAME# Operation:** G_FRAME# is an output when the GMCH acts as an initiator on the AGP Interface. G_FRAME# is asserted by the GMCH to indicate the beginning and duration of an access. G_FRAME# is an input when the GMCH acts as a FRAME#-based AGP target. As a FRAME#-based AGP target, the GMCH latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which GMCH samples FRAME# active.
IRDY#	**G_IRDY#: Initiator Ready.** **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_IRDY# is an output when GMCH acts as a FRAME#-based AGP initiator and an input when the GMCH acts as a FRAME#- based AGP target. The assertion of G_IRDY# indicates the current FRAME#-based AGP bus initiator's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_IRDY# indicates that the AGP-compliant master is ready to provide all write data for the current transaction. Once G_IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The master is never allowed to insert a wait state during the initial data transfer (32 bytes) of a write transaction. However, it may insert wait states after each 32-byte block is transferred.
TRDY#	**G_TRDY#:** Target Ready. **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_TRDY# is an input when the GMCH acts as an AGP initiator and is an output when the GMCH acts as a FRAME#-based AGP target. The assertion of G_TRDY# indicates the target's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_TRDY# indicates the AGP compliant target is ready to receive write data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on write transactions.
STOP#	**G_STOP#:** Stop. **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_STOP# is an input when the GMCH acts as a FRAME#-based AGP initiator and is an output when the GMCH acts as a FRAME#- based AGP target. G_STOP# is used for disconnect, retry, and abort sequences on the AGP interface.
DEVSEL#	**G_ DEVSEL#: Device Select.** **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_DEVSEL#, when asserted, indicates that a FRAME#-based AGP target device has decoded its address as the target of the current access. The GMCH asserts G_DEVSEL# based on the DDR SDRAM address range being accessed by a PCI initiator. As an input, G_DEVSEL# indicates whether the AGP master has recognized a PCI cycle to it.
REQ#	**G_REQ#:** Request. **During SBA Operation:** This signal is not used during SBA operation. **During PIPE# and FRAME# Operation:** G_REQ#, when asserted, indicates that the AGP master is requesting use of the AGP interface to run a FRAME#- or PIPE#-based operation.
GNT#	**G_GNT#: Grant.** **During SBA, PIPE# and FRAME# Operation:** G_GNT#, along with the information on the ST[2:0] signals (status bus), indicates how the AGP interface will be used next. Refer to the *AGP Interface Specification, Revision 2.0* for further explanation of the ST[2:0] values and their meanings.
AD[31:0]	**G_AD[31:0]: Address/Data Bus.** **During PIPE# and FRAME# Operation:** The G_AD[31:0] signals are used to transfer both address and data information on the AGP interface. **During SBA Operation:** The G_AD[31:0] signals are used to transfer data on the AGP interface.

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CBE#[3:0]	**Command/Byte Enable.** **During FRAME# Operation:** During the address phase of a transaction, the G_CBE[3:0]# signals define the bus command. During the data phase, the G_CBE[3:0]# signals are used as byte enables. The byte enables determine which byte lanes carry meaningful data. The commands issued on the G_CBE# signals during FRAME#-based AGP transactions are the same G_CBE# command described in the PCI 2.2 specification. **During PIPE# Operation:** When an address is enqueued using PIPE#, the C/BE# signals carry command information. The command encoding used during PIPE#- based AGP is *different* than the command encoding used during FRAME#-based AGP cycles (or standard PCI cycles on a PCI bus). **During SBA Operation:** These signals are not used during SBA operation.
PAR	**Parity.** **During FRAME# Operation:** G_PAR is driven by the GMCH when it acts as a FRAME#-based AGP initiator during address and data phases for a write cycle, and during the address phase for a read cycle. G_PAR is driven by the GMCH when it acts as a FRAME#-based AGP target during each data phase of a FRAME#-based AGP memory read cycle. Even parity is generated across G_AD[31:0] and G_CBE[3:0]#. **During SBA and PIPE# Operation:** This signal is not used during SBA and PIPE# operation.
Hub Interface signals	
HL[10:0]	**Packet Data:** Data signals used for HI read and write operations.
HLSTB	**Packet Strobe:** One of two differential strobe signals used to transmit or receive packet data over HI.
HLSTB#	**Packet Strobe Complement**: One of two differential strobe signals used to transmit or receive packet data over HI.
Clocks	
CLKIN	**Input Clock:** 66-MHz, 3.3-V input clock from external buffer DVO/Hub interface.
DVOBCLK **DVOBCLK#**	**Differential DVO Clock Output:** These pins provide a differential pair reference clock that can run up to 165-MHz. DVOBCLK corresponds to the primary clock out. DVOBCLK# corresponds to the primary complementary clock out. DVOBCLK and DVOBCLK# should be left as NC ("Not Connected") if the DVO B port is not implemented.
DVOCCLK **DVOCCLK#**	**Differential DVO Clock Output**: These pins provide a differential pair reference clock that can run up to 165-MHz. DVOCCLK corresponds to the primary clock out. DVOCCLK# corresponds to the primary complementary clock out. DVOCCLK and DVOCCLK# should be left as NC ("Not Connected") if the DVO C port is not implemented.
DVOBCCLKINT	**DVOBC Pixel Clock Input/Interrupt:** This signal may be selected as the reference input to either dot clock PLL (DPLL) or may be configured as an interrupt input. A TV-out device can provide the clock reference. The maximum input frequency for this signal is 85 -MHz. DVOBC Pixel Clock Input: When selected as the dot clock PLL (DPLL) reference input, this clock reference input supports SSC clocking for DVO LVDS devices. DVOBC Interrupt: When configured as an interrupt input, this interrupt can support either DVOB or DVOC. DVOBCCLKINT needs to be pulled down if the signal is NOT used.
DPMS	**Display Power Management Signaling:** This signal is used only in mobile systems to act as the DREFCLK in certain power management states(i.e. Display Power Down Mode); DPMS Clock is used to refresh video during S1-M. Clock Chip is powered down in S1-M. DPMS should come from a clock source that runs during S1-M and needs to be 1.5 V. So, an example would be to use a 1.5-V version of SUSCLK from ICH4-M.

4.5 Parallel ATA harddisk interface

Two parallel ATA harddisk controllers are available on the board – a primary and a secondary controller. Standard 3½" harddisks or CD-ROM drives may be attached to the primary and secondary controller board by means of the 40 pin IDC connectors, IDE_P and IDE_S.
The secondary controller is shared between the IDE_S connector and the IDE_S2 connector, which is intended for 2½" harddisks.
The harddisk controllers support Bus master IDE, ultra DMA 33/66/100 MHz and standard operation modes.

The signals used for the harddisk interface are the following:

Signal	Description
DA*2..0	Address lines, used to address the I/O registers in the IDE hard disk.
HDCS*1..0#	Hard Disk Chip-Select. HDCS0# selects the primary hard disk.
D*15..8	High part of data bus.
D*7..0	Low part of data bus.
IOR*#	I/O Read.
IOW*#	I/O Write.
IORDY*#	This signal may be driven by the hard disk to extend the current I/O cycle.
RESET*#	Reset signal to the hard disk. The signal is similar to RSTDRV in the PC-AT bus.
HDIRQ*	Interrupt line from hard disk. Routed by the SiS630 chipset to PC-AT bus interrupt.
CBLID*	This input signal (CaBLe ID) is used to detect the type of attached cable: 80-wire cable when low input and 40-wire cable when 5V via 10Kohm (pull-up resistor).
DDREQ*	Disk DMA Request might be driven by the IDE hard disk to request bus master access to the PCI bus. The signal is used in conjunction with the PCI bus master IDE function and is not associated with any PC-AT bus compatible DMA channel.
DDACK*#	Disk DMA Acknowledge. Active low signal grants IDE bus master access to the PCI bus.
HDACT*#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signals from primary and secondary controller are routed together through diodes and passed to the connector FEATURE.

All of the above signals are compliant to [4].
"*" is "A" for primary and "B" for secondary controller.
The pinout of the connectors are defined in the following sections.

4.5.1 IDE Hard Disk Connector (IDE_P)

This connector can be used for connection of two primary IDE drives.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESETA#	1	2	GND	PWR	-	-	
	-	TBD	IO	DA7	3	4	DA8	IO	TBD	-	
	-	TBD	IO	DA6	5	6	DA9	IO	TBD	-	
	-	TBD	IO	DA5	7	8	DA10	IO	TBD	-	
	-	TBD	IO	DA4	9	10	DA11	IO	TBD	-	
	-	TBD	IO	DA3	11	12	DA12	IO	TBD	-	
	-	TBD	IO	DA2	13	14	DA13	IO	TBD	-	
	-	TBD	IO	DA1	15	16	DA14	IO	TBD	-	
	-	TBD	IO	DA0	17	18	DA15	IO	TBD	-	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	-	-	I	DDRQA	21	22	GND	PWR	-	-	
	-	TBD	O	IOWA#	23	24	GND	PWR	-	-	
	-	TBD	O	IORA#	25	26	GND	PWR	-	-	
	4K7	-	I	IORDYA	27	28	GND	PWR	-	-	
	-	-	O	DDACKA#	29	30	GND	PWR	-	-	
	8K2	-	I	HDIRQA	31	32	NC	-	-	-	
	-	TBD	O	DAA1	33	34	CBLIDA#	I	-		
	-	TBD	O	DAA0	35	36	DAA2	O	TBD	-	
	-	TBD	O	HDCSA0#	37	38	HDCSA1#	O	TBD	-	
	-	-	I	HDACTA#	39	40	GND	PWR	-	-	

4.5.2 IDE Hard Disk Connector (IDE_S)

This connector can be used for connection of up till two secondary IDE drive(s), but only if no drive(s) is installed via IDE_S2 socket. The IDE_S is not available on the 886LCD-M/mITX.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESETB#	1	2	GND	PWR	-	-	
	-	TBD	IO	DB7	3	4	DB8	IO	TBD	-	
	-	TBD	IO	DB6	5	6	DB9	IO	TBD	-	
	-	TBD	IO	DB5	7	8	DB10	IO	TBD	-	
	-	TBD	IO	DB4	9	10	DB11	IO	TBD	-	
	-	TBD	IO	DB3	11	12	DB12	IO	TBD	-	
	-	TBD	IO	DB2	13	14	DB13	IO	TBD	-	
	-	TBD	IO	DB1	15	16	DB14	IO	TBD	-	
	-	TBD	IO	DB0	17	18	DB15	IO	TBD	-	
	-	-	PWR	GND	19	20	KEY	-	-	-	
	-	-	I	DDRQB	21	22	GND	PWR	-	-	
	-	TBD	O	IOWB#	23	24	GND	PWR	-	-	
	-	TBD	O	IORB#	25	26	GND	PWR	-	-	
	4K7	-	I	IORDYB	27	28	GND	PWR	-	-	
	-	-	O	DDACKB#	29	30	GND	PWR	-	-	
	8K2	-	I	HDIRQB	31	32	NC	-	-	-	
	-	TBD	O	DAB1	33	34	CBLIDB#	I	-		
	-	TBD	O	DAB0	35	36	DAB2	O	TBD	-	
	-	TBD	O	HDCSB0#	37	38	HDCSB1#	O	TBD	-	
	-	-	I	HDACTB#	39	40	GND	PWR	-	-	

4.5.3 IDE Hard Disk Connector (IDE_S2)

This connector (44-pin 2.0 mm pitch) can be used for connection of up till two secondary IDE drives, but only if no drive(s) is installed via IDE_S socket.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	TBD	O	RESETB#	1	2	GND	PWR	-	-	
	-	TBD	IO	DB7	3	4	DB8	IO	TBD	-	
	-	TBD	IO	DB6	5	6	DB9	IO	TBD	-	
	-	TBD	IO	DB5	7	8	DB10	IO	TBD	-	
	-	TBD	IO	DB4	9	10	DB11	IO	TBD	-	
	-	TBD	IO	DB3	11	12	DB12	IO	TBD	-	
	-	TBD	IO	DB2	13	14	DB13	IO	TBD	-	
	-	TBD	IO	DB1	15	16	DB14	IO	TBD	-	
	-	TBD	IO	DB0	17	18	DB15	IO	TBD	-	
	-	-	PWR	GND	19	20	NC	-	-	-	
	-	-	I	DDRQB	21	22	GND	PWR	-	-	
	-	TBD	O	IOWB#	23	24	GND	PWR	-	-	
	-	TBD	O	IORB#	25	26	GND	PWR	-	-	
	4K7	-	I	IORDYB	27	28	GND	PWR	-	-	
	-	-	O	DDACKB#	29	30	GND	PWR	-	-	
	8K2	-	I	HDIRQB	31	32	NC	-	-	-	
	-	TBD	O	DAB1	33	34	CBLIDB#	I			
	-	TBD	O	DAB0	35	36	DAB2	O	TBD	-	
	-	TBD	O	HDCSB0#	37	38	HDCSB1#	O	TBD	-	
	-	-	I	HDACTB#	39	40	GND	PWR	-	-	
	-	-	PWR	VCC	41	42	VCC	PWR	-	-	
	-	-	PWR	GND	43	44	NC	-	-	-	

4.5.4 CF Connector (CF)

This connector is mounted on the backside of the 886LCD-M/mITX only. If a Compact Flash Disk is used, then no IDE drive can be connected to the IDE_S2 connector. The socket support DMA/UDMA modules.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
2	-	-	-	NC	26	1	GND	PWR	-	-	1
	-	TBD	IO	DB11	27	2	DB3	IO	TBD	-	
	-	TBD	IO	DB12	28	3	DB4	IO	TBD	-	
	-	TBD	IO	DB13	29	4	DB5	IO	TBD	-	
	-	TBD	IO	DB14	30	5	DB6	IO	TBD	-	
	-	TBD	IO	DB15	31	6	DB7	IO	TBD	-	
	-	TBD	O	HDCSB#	32	7	HDCSB0#	O	TBD	-	
	-	-	-	NC	33	8	GND	PWR	-	-	
	-	TBD	O	IORB#	34	9	GND	PWR	-	-	
	-	TBD	O	IOWB#	35	10	GND	PWR	-	-	
	-	-	PWR	5V	36	11	GND	PWR	-	-	
	8K2	-	I	IRQB	37	12	GND	PWR	-	-	
	-	-	PWR	5V	38	13	5V	PWR	-	-	
	-	-	PWR	GND	39	14	GND	PWR	-	-	
	-	-	-	NC	40	15	GND	PWR	-	-	
	-	TBD	O	RESETB#	41	16	GND	PWR	-	-	
	4K7	-	I	IORDYB#	42	17	GND	PWR	-	-	
	-	-	I	DDREQB	43	18	DAB2	O	-	-	
	-	-	O	DDACKB#	44	19	DAB1	O	-	-	
	-	-	I	DASP	45	20	DAB0	O	-	-	
	-	-	I	PDIAG	46	21	DB0	IO	TBD	-	
	-	TBD	IO	DB8	47	22	DB1	IO	TBD	-	
	-	TBD	IO	DB9	48	23	DB2	IO	TBD	-	
	-	TBD	IO	DB10	49	24	NC				
1	-	-	PWR	GND	50	25	NC	-	-	-	2

Note 1: Pin is longer than average length of the other pins.
Note 2: Pin is shorter than average length of the other pins.

4.6 Serial ATA harddisk interface

Two serial ATA harddisk controllers are available on the board – a primary controller (SATA0) and a secondary controller (SATAB).

4.6.1 SATA Hard Disk Connector (SATA0, SATA1)

SATA0:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
Key					
1	GND	PWR	-	-	
2	SATA0 TX+				
3	SATA0 TX-				
4	GND	PWR	-	-	
5	SATA0 RX-				
6	SATA0 RX+				
7	GND	PWR	-	-	

The signals used for the primary Serial ATA harddisk interface are the following:

Signal	Description
SATA0 RX+ SATA0 RX-	Host transmitter differential signal pair
SATA0 TX+ SATA0 TX-	Host receiver differential signal pair

All of the above signals are compliant to [4].

SATA1:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
Key					
1	GND	PWR	-	-	
2	SATA1 TX+				
3	SATA1 TX-				
4	GND	PWR	-	-	
5	SATA1 RX-				
6	SATA1 RX+				
7	GND	PWR	-	-	

The signals used for the secondary Serial ATA harddisk interface are the following:

Signal	Description
SATA1 RX+ SATA1 RX-	Host transmitter differential signal pair
SATA1 TX+ SATA1 TX-	Host receiver differential signal pair

All of the above signals are compliant to [4].

4.7 Printer Port Connector (PRINTER).

The printer port connector is provided in a standard DB25 pinout.
The signal definition in standard printer port mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1						
						14	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	2						
						15	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	3						
						16	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	4						
						17	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	5						
						18	GND	PWR	-	-	
	2K2	24/24	IO	PD4	6						
						19	GND	PWR	-	-	
	2K2	24/24	IO	PD5	7						
						20	GND	PWR	-	-	
	2K2	24/24	IO	PD6	8						
						21	GND	PWR	-	-	
	2K2	24/24	IO	PD7	9						
						22	GND	PWR	-	-	
	2K2	-	I	ACK#	10						
						23	GND	PWR	-	-	
	2K2	-	I	BUSY	11						
						24	GND	PWR	-	-	
	2K2	-	I	PE	12						
						25	GND	PWR	-	-	
	2K2	-	I	SLCT	13						

The interpretation of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

Signal	Description
PD7..0	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD7..0 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Signal from printer indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initializes (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode as defined in [3].

4.8 Serial Ports

Four RS232C serial ports are available on the 886LCD-M/Flex, 886LCD-M/ATX and 886LCD-M/mITX.

The typical interpretation of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitte Data, sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Receive Data, receives serial data from the communication link.
DTR	Data Terminal Ready, indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send, indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a telephone-ringing signal.

The connector pinout for each operation mode is defined in the following sections.

4.8.1 Com1 (Port1) DB9 Connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5	9	RI	I	-	/5K	
	-		O	DTR	4	8	CTS	I	-	/5K	
	-		O	TxD	3	7	RTS	O		-	
	/5K	-	I	RxD	2	6	DSR	I	-	/5K	
	/5K	-	I	DCD	1						

4.8.2 Com2, Com3 & Com4 Pin Header Connectors.

The pinout of Serial ports Com2 (Port2), Com3 (SIO Port1) and Com4 (SIO Port2) is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1	2	DSR	I	-		
		-	I	RxD	3	4	RTS	O		-	
	-		O	TxD	5	6	CTS	I	-		
	-		O	DTR	7	8	RI	I	-		
	-	-	PWR	GND	9	10	5V	PWR	-	-	1

Note 1: 5V supply is shared with supply pins in Com2/Com3/Com4 headers. The common fuse is 1.1A.

If the DB9 adapter (ribbon cable) is used, the DB9 pinout will be identical to the pinout of Serial Com1

4.9 Ethernet connectors.

The 886LCD-M/Flex, 886LCD-M/ATX and 886LCD-M/mITX boards supports 3 channels of 10/100/1000Mb Ethernet.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

The signals for the Ethernet ports are as follows:

Signal	Description
MDI[0]+ MDI[0]-	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]+ MDI[1]-	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[2]+ MDI[2]-	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[3]+ MDI[3]-	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.

Note: MDI = Media Dependent Interface.

4.9.1 Ethernet connector 1 (ETHER1)

Ethernet connector 1 is mounted together with USB Ports 0 and 2.

The pinout of the RJ45 connector is as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+				
MDI0-				
MDI1+				
MDI2+				
MDI2-				
MDI1-				
MDI3+				
MDI3-				
	8 7 6 5 4 3 2 1			

4.9.2 Ethernet connector 2/3 (ETHER2/3)

The two Ethernet channels in ETHER2/3 are supported by two discrete Ethernet controllers connected to the onboard PCI bus.

This connector is not supported on the Engineering sample boards.

The pinout of the RJ45's connector are as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+	1			
MDI0-	2			
MDI1+	3			
MDI2+	4			
MDI2-	5			
MDI1-	6			
MDI3+	7			
MDI3-	8			
	8 7 6 5 4 3 2 1			
	1 2 3 4 5 6 7 8			
MDI0+	1			
MDI0-	2			
MDI1+	3			
MDI2+	4			
MDI2-	5			
MDI1-	6			
MDI3+	7			
MDI3-	8			

Note: The connector has two LEDs which indicates connection and traffic status. The left LED is status for the ETHER3 (buttom port) and the right LED is for ETHER2. More than one type of connector is approved for this application. Please notice that it is possible that the shape of the LED might vary depending on actual type of connector.

4.10 USB Connector (USB)

The 886LCD-M/Flex, 886LCD-M/ATX and 886LCD-M/mITX contains two USB (Universal Serial Bus) ports UHCI Host Controllers. Each Host Controller includes a root hub with two separate USB ports each, for a total of 4 USB ports.

The USB Host Controllers support the standard Universal Host Controller Interface (UHCI) Specification, Rev 1.1. All 4 USB ports support both USB1.0 and USB2.0 signaling and all ports supports Legacy mode. (See chapter “Legacy USB Support” for more info).

Over-current detection on all four USB ports is supported.

USB Port 0 and 2 are supplied on the combined ETHER1, USB0, USB2 connector. USB Ports 1 and 3 are supplied on the FRONTPNL connector; please refer to the FRONTPNL connector section for the pin-out.

4.10.1 USB Connector 0/2 (USB0/2)

USB Ports 0 and 2 are mounted together with ETHER1 ethernet port.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB0-		USB0+	IO	0.25/2	/15K	
					1 2 3 4					
1	-	-	PWR	5V/SB5V		GND	PWR	-	-	
	/15K	0.25/2	IO	USB2-		USB2+	IO	0.25/2	/15K	

Note 1: The 5V supply for the USB devices is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity. In order to meet the requirements of USB v.1.1 standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB0+ USB0- USB2+ USB2-	Differential pair works as Data/Address/Command Bus.
USB5V	5V supply for external devices. Fused with 1.5A reset-able fuse.

4.11 Audio Connector

4.11.1 Audio Line-in, Line-out and Microphone

Audio Line-in, Line-out and Microphone are available in the stacked audio jack connector.

IN	Signal	Type	Note
TIP	Line in – Left	IA	1
RING	Line in – Right	IA	1
SLEEVE	GND	PWR	
TIP	Line out – Left	OA	
RING	Line out – Right	OA	
SLEEVE	GND	PWR	
TIP	MIC 1	IA	1, 2
RING	MIC 2	IA	1, 2
SLEEVE	GND	PWR	2

Note 1: Signals are shorted to GND internally in the connector, when jack-plug not inserted.
Note 2: Microphone is not supported on Engineering board samples

4.11.2 CD-ROM Audio input (CDROM)

CD-ROM audio input may be connected to this connector. It may also be used as a secondary line-in signal.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CD_Left	IA	-	-	1
2	CD_GND	IA	-	-	
3	CD_GND	IA	-	-	
4	CD_Right	IA	-	-	1

Note 1: The definition of which pins are use for the Left and Right channels is not a worldwide accepted standard. Some CDROM cable kits expect reverse pin order.

Signal	Description
CD_Left CD_Right	Left and right CD audio input lines or secondary Line-in.
CD_GND	Analogue GND for Left and Right CD. (This analogue GND is **not** shorted to the general digital GND on the board).

4.11.3 AUDIO Header (AUDIO_HEAD)

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN	PIN	Signal	Type	Ioh/ Iol	Pull U/D	Note
				AMP-LFE-OUT	1	2	AMP-CEN-OUT				
				AAGND	3	4	AAGND				
				SPKR_OUT_L	5	6	SPKR_OUT_R				
				AAGND	7	8	AAGND				
				SURR-OUT-L	9	10	SURR-OUT-R				
				NC	11	12	NC				
				AAGND	13	14	AAGND				
				F-FRONT-MIC1	15	16	F-FRONT-MIC2				
				AAGND	17	18	AAGND				
				F-AUX-IN-L	19	20	F-AUX-IN-R				
				F-MONO-OUT	21	22	AAGND				
	-	-	PWR	GND	23	24	F-SPDIF-IN				
				F-SPDIF-OUT	25	26	GND	PWR	-	-	

Signal	Description	Amplifier	Note
SPKR_OUT_L	Front Speakers (Speaker Out Left).	3W	
SPKR_OUT_R	Front Speakers (Speaker Out Right).	3W	
SURR-OUT-L	Rear Speakers (Surround Out Left).	no	Select 4 or 5.1 speakers **
SURR-OUT-R	Rear Speakers (Surround Out Right).	no	Select 4 or 5.1 speakers **
AMP-CEN-OUT	Center Speaker (Center Out channel).	3W *	Select 5.1 speakers **
AMP-LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	3W *	Select 5.1 speakers **
F-MONO-OUT	Speaker Phone Output	no	
NC	No connection	---	
F-FRONT-MIC1	Dedicated MIC Input 1 for Frontpanel MIC	---	
F-FRONT-MIC2	Dedicated MIC Input 2 for Frontpanel MIC	---	
F-AUX-IN-L	AUX Left Channel input	---	
F-AUX-IN-R	AUX Right Channel input	---	
F-SPDIF-IN	S/PDIF Input	---	
F-SPDIF-OUT	S/PDIF Output	---	Enable SPDIF ***
AAGND	Audio Analogue ground	---	

* Not amplified on 886LCD-M/mITX.
** In the Realtek Audio Driver
*** In the Realtek Audio Driver (XP only). Also enable SPDIF in Player (if used).

4.12 Fan connectors , FAN_PROC and FAN_SYS.

The **FAN_PROC** is used for connection of the active cooler for the CPU.

The **FAN_SYS** can be used to power, control and monitor a fan for chassis ventilation etc.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	SENSE	PWR	-	4K7	
2	12V	PWR	-	-	
3	GND	PWR	-	-	

Signal description:

Signal	Description
12V	+12V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 800 mA can be supplied from this pin.
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. On board is a pull-up resistor 4K7 to +12V. The signal has to be pulses, typically 2 Hz per rotation.

4.13 The Clear CMOS Jumper, Clr-CMOS.

The Clr-CMOS Jumper is used to clear the CMOS content.

↑ CPU location ↑

No Jumper installed	1 2 3	(Pin numbers)
Jumper normal position	[1-2 jumpered] •	
Jumper in Clear CMOS position	• [2-3 jumpered]	

To clear all CMOS settings, including Password protection, move the CMOS_CLR jumper (with or without power on the system) for approximately 1 minute.

Alternatively if no jumper is available, turn off power and remove the battery for 1 minute, but be careful to orientate the battery corretly when reinserted.

4.14 LPC connector (unsupported).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	1	2	LPCCLK				
	-	-	PWR	GND	3	4	LPC AD0				
				LPC FRAME#	5	6	LPC AD1				
				INT SERIQ	7	8	LPC AD2				
				LPC DRQ#1	9	10	LPC AD3				

4.15 Front Panel connector (FRONTPNL).

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
				USB13_5V	1	2	USB13_5V				
				USB1-	3	4	USB3-				
				USB1+	5	6	USB3+				
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-	-	NC	9	10	NC	-	-	-	
	-	-	PWR	+5V	11	12	+5V	PWR	-	-	
			OC	HD_LED	13	14	SUS_LED				
	-	-	PWR	GND	15	16	PWRBTN_IN#				
				RSTIN#	17	18	GND	PWR	-	-	
				SB3V3	19	20	NC	-	-	-	
				AGND	21	22	AGND				
				SPKR_OUT_L	23	24	SPKR_OUT_R				

Signal	Description
USB13_5V	+5V supply for the USB devices on USB Port 1 and 3 is on-board fused with a 1.5A reset-able fuse. The supply is common for the two channels. SB5V is supplied during power down to allow wakeup on USB device activity.
USB1+ USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
USB3+ USB3-	Universal Serial Bus Port 3 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A or 2A per pin if using IDC connectorfladkabel or crimp terminals respectively.
HD_LED	Hard Disk Activity LED (active low signal). Output is via 475Ω to OC.
SUS_LED	Suspend Mode LED (active high signal). Output is via 475Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX PSU and boot the board.
RSTIN#	Reset Input. Pull low to reset the board.
SPKR_OUT_L	Speaker Out Left channel, amplified, 3W
SPKR_OUT_R	Speaker Out Right channel, amplified, 3W
SB3V3	Standby 3.3V voltage
AGND	Analogue Ground for Audio

4.16 Intruder Connector (INT)

This connector is available on the 886LCD-M/Flex only, however please notice that the INTRUDER function is also available on the Feature connector.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	GND	PWR	-	-	
2	INTRUDER#	I	-	100K	
3	GND	PWR	-	-	

INTRUDER detect: May be used to detect if the system case has been opened.
This signal's status is readable, so it may be used like a GPI when the Intruder switch is not needed.

4.17 Feature Connector (FEATURE)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
2	100K/	-	I	INTRUDER#	1	2	GND	PWR	-	-	
				EXT_ISAIRQ#	3	4	EXT_SMI#	I			
				PWR_OK	5	6	SB5V	PWR	-	-	
	-	-	PWR	SB3V3	7	8	EXT_BAT	PWR	-	-	
	-	-	PWR	+5V	9	10	GND	PWR	-	-	
			IOT	GPIO0	11	12	GPIO1	IOT			
			IOT	GPIO2	13	14	GPIO3	IOT			
			IOT	GPIO4	15	16	GPIO5	IOT			
			IOT	GPIO6	17	18	GPIO7	IOT			
	-	-	PWR	GND	19	20	FAN3OUT				
				FAN3IN	21	22	+12V	PWR	-	-	
				TEMP3IN	23	24	VREF				
	-	-	PWR	GND	25	26	IRRX				
				IRTX	27	28	GND	PWR	-	-	
1	2K7/			SMBC	29	30	SMBD			2K7/	1

Note 1: Pull-up to 3V3 supply
Note 2: Pull-up to RTC-Voltage

Signal	Description
INTRUDER#	INTRUDER, may be used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not needed.
EXT_ISAIRQ#	EXTernal ISA IRQ, (active low input) can activate standard AT-Bus IRQ-interrupt.
EXT_SMI#	External SMI, (active low input) signal can activate SMI interrupt.
PWR_OK	PoWeR OK, signal is high if no power failures is detected.
SB5V	StandBy +5V supply.
SB3V3	Standby 3.3V. Max. load is 0.75A (1.5A < 1 sec.)
EXT_BAT	(EXTernal BATtery) the + terminal of an external primary cell battery can be connected to this pin. The – terminal of the battery shall be connected to GND (etc. pin 10). The external battery is protected against charging and can be used with or without the on board battery installed. The external battery voltage shall be in the range: 2.5 - 4.0 V DC.
+5V	Max. load is 0.75A (1.5A < 1 sec.)
GPIO0..7	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KONTRON API (Application Programming Interface) available for Win98, WinXP and Win2000.
FAN3OUT	FAN 3 speed control OUTput. This analogue voltage output signal can be used to control the Fan's speed. The output has 16 values in the range from 0 – 5V. For more information please look into the datasheet for the Winbond I/O controller W83627.
FAN3IN	FAN3 Input. 0V to +5V amplitude Fan 3 tachometer input.
+12V	Max. load is 0.75A (1.5A < 1 sec.)
TEMP3IN	Temperature sensor 3 input. (Recommended: Transistor 2N3904, having emitter connected to GND (pin 25), collector and basis shorted and connected to pin23 (Temp3-In). Further a resistor 30K/1% shall be connected between pin 23 and pin 24 (Vref).
VREF	Voltage REFerence, reference voltage to be used with TEMP3IN input.
IRRX	IR Receive input (IrDA 1.0, SIR up to 1.152K bps)
IRTX	IR Transmit output (IrDA 1.0, SIR up to 1.152K bps)
SMBC	SMBus Clock signal
SMBD	SMBus Data signal

4.17.1 PCI Slot Connector

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
	I	TDO	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
	I	REQ2#	F09	E09	CLKC	O	
	I	REQ3#	F10	E10	+5V (I/O)	PWR	
	OT	GNT2#	F11	E11	CLKD	O	
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
	O	CLKA	F14	E14	GNT3#	OT	
	PWR	GND	F15	E15	RST#	O	
	O	CLKB	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0#	OT	
	I	REQ0#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	REQ1#	I	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	GNT1#	OT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SDONE	IO	
	PWR	+3.3V	F41	E41	SB0#	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
		SOLDER SIDE			**COMPONENT SIDE**		
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
	IOT	ACK64#	F60	E60	REQ64#	IOT	
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

4.17.2 Signal Description –PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33 MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

(continues)

ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted.
	While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

4.17.3 886LCD-M PCI IRQ & INT routing

Board type	Slot	IDSEL	INTA	INTB	INTC	INTD
886LCD-M/mITX	1	AD16	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H
886LCD-M/FLEX	1	AD16	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H
	2	AD17	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E
	3	AD18	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E	INT_PIRQ#F
886LCD-M/ATX	1	AD16	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H
	2	AD17	INT_PIRQ#F	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E
	3	AD18	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E	INT_PIRQ#F
	4	AD19	INT_PIRQ#H	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G
	5	AD20	INT_PIRQ#D	INT_PIRQ#C	INT_PIRQ#B	INT_PIRQ#A
	6	AD21	INT_PIRQ#C	INT_PIRQ#B	INT_PIRQ#A	INT_PIRQ#D

When using the 820982 “PCI Riser - Flex - 2slot w. arbiter” the BIOS option “PCI riser Support” shall be disabled. Then the lower slot has IDSEL / IRQs routed straight through and the top slot has the routing: IDSEL=AD22, INT_PIRQ#F, INT_PIRQ#G, INT_PIRQ#H, INT_PIRQ#E. 820982 PCI Riser shall be plugged into Slot #1.

The BIOS option of “PCI riser Support” is for support of another type of dual PCI Riser module having one PCI slot IDSEL / IRQs signals routed straight through and the other PCI slot routing: IDSEL=AD19, INT_PIRQ#H, INT_PIRQ#E, INT_PIRQ#F, INT_PIRQ#G. Such a Riser card to be is not available from Kontron at present time.

5. Onboard Connectors

Connector	Onboard Connectors		Mating Connectors	
	Manufacturer	Type no.	Manufacturer	Type no.
FAN_SYS,	Molex	22-23-2031	AMP	1375820-3
FAN_PROC				
INT				
KBDMSE	Molex	22-23-2061	Molex	22-01-2065
CDROM	Foxconn	HF1104E	Molex	50-57-9404
	Molex	70543-0038		
SATA0	Molex	67491-0020	Molex	67489-8005
SATA1			Kontron	KT 821035 (cable kit)
ATXPWR	FoxConn	HM2510E	Molex	39-01-2205
COM2	Foxconn	HL20051	Molex	90635-1103
COM3			Kontron	KT 821016 (cable kit)
COM4			Kontron	KT 821017 (cable kit)
AUDIO_HEAD	Molex	87831-2620	Molex	51110-2651
			Kontron	KT 821043 (cable kit)
			Kontron	KT 821044 (cable kit)
FRONTPNL	Foxconn	HL20121	Molex	90635-1243
			Kontron	KT 821042 (cable kit)
FEATURE	Molex	87831-3020	Molex	51110-3051
			Kontron	KT 821041 (cable kit)
IDE_P	Foxconn	HL20201-UD2	Kontron	KT 821018 (cable kit)
IDE_S			Kontron	KT 821013 (cable kit)
IDE_S2	Foxconn	HS5522V	AMP	2-111623-5
			Kontron	KT 821010 (cable kit)
			Kontron	KT 821012 (cable kit)
LVDS	Don Connex	C44-40BSB1-G	Don Connex	A32-40-C-G-B-1
			Kontron	KT 821515 (cable kit)
			Kontron	KT 821155 (cable kit)

6. System Ressources

6.1 Memory map

Address range (hex)		Size	Description
00000000-	0007FFFF	512 Kbytes	Conventional memory
00080000-	0009FBFF	127 Kbyte	Extended conventional memory
0009FC00-	0009FFFF	1 Kbyte	Extended BIOS data
000A0000-	000AFFFF	64 Kbytes	885GME VGA Controller, Video memory and BIOS
000B0000-	000BFFFF	64 Kbytes	885GME VGA Controller, Video memory and BIOS
000C0000-	000CC5FF	49 Kbytes	885GME VGA Controller, Video memory and BIOS
000CC800-	000CD7FF	4 Kbytes	Realtek 8110 Ethernet Controller
D0000000-	DFFFFFFF	0xFFFFFFF	885GME Processor I/O Controller
E8000000-	EFFFFFFF	0x7FFFFFF	885GME VGA Controller
F0000000-	F7FFFFFF	0x7FFFFFF	885GME VGA Controller
FF7FF400-	FF7FF4FF	0xFF	Realtek 8110 Ethernet Controller
FF7FF800-	FF7FF8FF	0xFF	Realtek 8110 Ethernet Controller
FF7FFC00-	FF7FFCFF	0xFF	Realtek 8110 Ethernet Controller
FF980000-	FF9FFFFF	0x7FFFF	885GME VGA Controller
FFA7B000-	FFA7B00F	0xF	PCI System Peripheral
FFA7B400-	FFA7B7FF	0x3FF	USB Controller
FFA7B800-	FFA7B8FF	0xFF	Realtek AC97 Audio
FFA7BC00-	FFA7BDFF	0x1FF	Realtek AC97 Audio
FFA7FC00-	FFAFFFFF	0x803FF	Ultra SATA Controller
FFA80000-	FFAFFFFF	0x7FFFF	885GME VGA Controller
FFB00000-	FFEFFFFF	0x3FFFFF	Intel 82802 Firmware Hub Device
FFF00000-	FFFFFFFF	1 Mbyte	Intel 82802 Firmware Hub Device

6.2 PCI devices

Bus #	Device #	Function #	Vendor ID	Device ID	IDSEL	Chip	Device Function
0	0	0	8086h	3580h	AD11	6300ESB	Host bridge
0	0	1	8086h	3584h		6300ESB	I/O Controller
0	0	3	8086h	3585h		6300ESB	I/O Controller
0	1	0	8086h	3581h	AD12	6300ESB	Pci to Pci bridge
0	2	0	8086h	3582h	AD13	6300ESB	VGA controller
0	2	1	8086h	3582h		6300ESB	Display controller
0	28	0	8086h	25AEh	AD39	6300ESB	Pci to Pci bridge
0	29	0	8086h	25A9h	AD40	6300ESB	USB
0	29	1	8086h	25AAh		6300ESB	USB
0	29	4	8086h	25ABh		6300ESB	Watchdog timer
0	29	5	8086h	25ACh		6300ESB	APIC
0	29	7	8086h	25ADh		6300ESB	USB
0	30	0	8086h	244Eh	AD41	6300ESB	Pci to Pci bridge
0	31	0	8086h	25A1h	AD42	6300ESB	ISA Bridge
0	31	1	8086h	25A2h		6300ESB	IDE Controller
0	31	2	8086h	25A3h		6300ESB	IDE Controller
0	31	3	8086h	25A4h		6300ESB	SMBus
0	31	5	8086h	25A6h		6300ESB	Audio
0	*	-	-	-	*	-	PCI slot #1
0	*	-	-	-	*	-	PCI slot #2
0	*	-	-	-	*	-	PCI slot #3
0	*	-	-	-	*	-	PCI slot #4
2	1	0	10ECh	8169h	AD12	RTL8110	Ethernet
2	2	0	10ECh	8169h	AD13	RTL8110	Ethernet
2	3	0	10ECh	8169h	AD14	RTL8110	Ethernet

* Values are dynamically selected in BIOS.
Note: All PCI slots for the 886LCD-M boards supports PCI BUS Mastering.

6.3 Interrupt Usage

IRQ	Onboard system parity errors and IOCHCHK signal activation	Onboard Timer 0 Interrupt	Onboard Keyboard Interrupt	Used for Cascading IRQ8-IRQ15	May be used by onboard Serial Port A	May be used by onboard Serial Port B / IrDA Port	May be used by onboard Serial Port C	May be used by onboard Serial Port D	May be used by onboard SATA controller	May be used by onboard Parallel Port	May be used by onboard Floppy disk Controller	Used by onboard Real Time Clock Alarm	May be used by onboard P/S 2 support	Used for Onboard co-processor support	May be used by primary harddisk controller	May be used by secondary harddisk controller	May be used for onboard Sound System	May be used by onboard USB controller	May be used by onboard Ethernet controller 1	May be used by onboard Ethernet controller 2	May be used by onboard Ethernet controller 3	May be used by onboard VGA Controller	May be used by onboard SMBus Controller	Available on PCI slots as IRQA-IRQD depending on selections in the BIOS	Notes
NMI	•																								
IRQ0		•																							
IRQ1			•																						
IRQ2				•																					
IRQ3					•	•	•	•																•	1, 2
IRQ4					•	•	•	•																•	1, 2
IRQ5										•													•	•	1, 2
IRQ6					•	•	•	•			•													•	1, 2
IRQ7										•														•	1, 2
IRQ8												•													
IRQ9																		•	•	•	•			•	1, 2
IRQ10					•	•	•	•									•							•	1, 2
IRQ11					•	•	•	•																•	1, 2
IRQ12													•											•	1
IRQ13														•											
IRQ14															•									•	1
IRQ15																•								•	1
IRQ16																		•				•			3
IRQ17												•													3
IRQ18									•																3
IRQ19																		•							3
IRQ20																									3
IRQ21																									3
IRQ22																									3
IRQ23																		•							3
IRQ24																			•						3
IRQ25																				•					3
IRQ26																					•				3

Notes:

1. Availability of the shaded IRQs depends on the setting in the BIOS. According to the PCI Standard, PCI Interrupts IRQA-IRQD can be shared.
2. These interrupt lines are managed by the PnP handler and are subject to change during system initialisation.
3. IRQ16 to IRQ26 are APIC interrupts

6.4 I/O Map

Address (hex)	Size	Description
0020- 0021	1	Programmable interrupt controller
0040- 0043	4	System Timer
0060- 0060	1	Standard keyboard
0061- 0061	1	System speaker
0070- 0071	2	System CMOS/Real time clock
0170- 01F7	8	Secondary Parallel ATA IDE Channel
01F0- 01F7	8	Primary Parallel ATA IDE Channel
02E8- 02EF	8	Comport 4
02F8- 02FF	8	Comport 2
0378- 037F	8	Printer Port
03B0- 03BB	12	855GME VGA Controller
03C0- 03DF	32	855GME VGA Controller
03E8- 03EF	8	Comport 3
03F8- 03FF	8	Comport 1
0CF8- 0CFF	8	PCI Bus
D000- D0FF	256	Realtek 8169 Ethernet Controller
D000- DFFF	4096	PCI standard PCI-to-PCI brigde
D400- D4FF	256	Realtek 8169 Ethernet Controller
D800- D8FF	256	Realtek 8169 Ethernet Controller
E000- E01F	32	Standard Universal PCI to USB Host Controller
E080- E09F	32	Standard Universal PCI to USB Host Controller
E400- E41F	32	PCI System Management Bus
E480- E4BF	32	Realtek AC97 Audio
E800- E8FF	256	Realtek AC97 Audio
EC00- EC07	8	855GME VGA Controller
FC00- FC07	8	Primary Serial ATA IDE Channel
FC08- FC0F	8	Secondary Serial ATA IDE Channel

6.5 DMA Channel Usage

DMA Channel Number	Data Width	System Ressources
0	8 or 16 bits	Available
1	8 or 16 bits	Available
2	8 or 16 bits	Available
3	8 or 16 bits	Available
4	8 or 16 bits	DMA Controller
5	16 bits	Available
6	16 bits	Available
7	16 bits	Available

7. Overview of BIOS features

This Manual section details specific BIOS features for the 886LCD-M boards.
The 886LCD-M boards are based on the AMI BIOS core version 8.10 with Kontron BIOS extensions.

7.1 System Management BIOS (SMBIOS / DMI)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.

The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS.

The BIOS stores and reports the following SMBIOS information:
- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

The 886LCD-M Boards supports reading certain MIF specific details by the Windows API. Refer to the API section in this manual for details.

7.2 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

8. BIOS Configuration / Setup

8.1 Introduction

The BIOS Setup is used to view and configure BIOS settings for the 886LCD-M board. The BIOS Setup is accessed by pressing the DEL key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The Menu bar look like this:

```
                              BIOS SETUP UTILITY
   Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
```

The available keys for the Menu screens are:

Select Menu: <←> or <→>
Select Item: <↑> or <↓>
Select Field: <Tab>
Change Field: <+> or <->
Help: <F1>
Save and Exit: <F10>
Exits the Menu: <Esc>

8.2 Main Menu

```
                              BIOS SETUP UTILITY
   Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
   System Overview                                          Use [ENTER], [TAB] or
                                                            [SHIFT-TAB] to select
   AMIBIOS                                                  a field.
   Version    : 08.00.10
   Build Date: 11/17/08                                     Use [+] or [-] to
   ID         : 886LCD46                                    configure system Time.
   PCB ID     : 14
   Serial #   : 00374708
   PCB ID     : 63650000

   Processor
   Type       : Intel(R) Pentium(R) M Processor 1600 MHz   <-    Select Screen
   Speed      : 600MHz                                      ||    Select Item
                                                            +-    Change Field
   System Memory                                            Tab   Select Field
   Size       : 1016MB                                      F1    General Help
   Speed      : 333MHz                                      F10   Save and Exit
                                                            ESC   Exit
   System Time                      [10:18:15]
   System Date                      [Wed 26/11/2008]
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```

Note on "Speed": If the actual processor support Speed Step (Pentium M does) then BIOS will run at minimum Speed until BIOS is almost booted and then speed switch as selected for the "Intel Speed Tech" setting. Celeron M do not support Speed Step and therefore the Processor Speed will be fixed and identical to the clock speed listed for the Processor.

Main Menu Selections

You can make the following selections. Use the sub menus for other selections.

Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.

8.3 Advanced Menu

```
                         BIOS SETUP UTILITY
   Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
   Advanced Settings                                     | Configure CPU.
                                                         |
   Warning: Setting wrong values in below sections       |
            May cause system to malfunction.             |
                                                         |
>  CPU Configuration                                     |
>  IDE Configuration                                     |
>  LAN Configuration                                     |
>  Floppy Configuration                                  |
>  SuperIO Configuration                                 |
>  Hardware Health Configuration                         |
>  Voltage Monitor                                       | <-     Select Screen
>  ACPI Configuration                                    | ||     Select Item
>  Remote Access Configuration                           | Enter  Go to Sub Screen
>  USB Configuration                                     | F1     General Help
                                                         | F10    Save and Exit
                                                         | ESC    Exit
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```

8.3.1 Advanced settings – CPU Configuration

```
                         BIOS SETUP UTILITY
                 Advanced
   Configure advanced CPU settings                       | Maximum: CPU Speed is
   Module Version – 11.05                                | set to maximum.
                                                         | Minimum: CPU Speed is
   Manufacturer: Intel                                   | set to minimum.
   Brand String: Intel (R) Pentium(R) M processor 1600M  | Automatic: CPU speed
   Frequency    : 600MHz                                 | controlled by
   FSB Speed    : 400MHz                                 | Operating system.
                                                         | Disabled: Default CPU
   Cache L1     : 32 KB                                  | speed.
   Cache L2     : 1024 KB                                |
                                                         |
   Intel(R) SpeedStep(tm) tech.    [Automatic]           | <-     Select Screen
                                                         | ||     Select Item
                                                         | +-     Change Option
                                                         | F1     General Help
                                                         | F10    Save and Exit
                                                         | ESC    Exit
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```

Feature	Options	Description
Intel(R) SpeedStep(tm) tech.	Maximum Speed, Minimum Speed, Automatic, Disabled	Select the operation mode of the CPU. To ensure full performance of the CPU, use the Maximum Speed setting.

8.3.2 Advanced settings – IDE Configuration

```
                          BIOS SETUP UTILITY
           Advanced
   IDE Configuration                                        | Select IDE Mode.
   IDE Configuration               [P-ATA Only]             |
    S-ATA Running Enhanced         [Yes]                    | P-ATA Only:
     P-ATA Channel Selection       [Both]                   |   4 P-ATA & 2 S-ATA
     S-ATA Ports Definition        [P0-3rd./P1-4th]         |
     Configure S-ATA as RAID       [No]                     | S-ATA Only:
                                                            |   2 S-ATA
   Primary IDE Master                 : [Hard Disk]         |
   Primary IDE Slave                  : [Not Detected]      | P-ATA & S-ATA
   Secondary IDE Master               : [Not Detected]      |   2 P-ATA & 2 S-ATA
   Secondary IDE Slave                : [Not Detected]      |
   Third IDE Master                   : [Not Detected]      |
   Third IDE Slave                    : [Not Detected]      |
   Fourth IDE Master                  : [Not Detected]      | <-     Select Screen
   Fourth IDE Slave                   : [Not Detected]      | ||     Select Item
                                                            | +-     change option
   ATA(PI) 80Pin Cable Detection   [Host & Device]          | F1     General Help
   P-ATA1 Cable Detection force    [Disabled]               | F10    Save and Exit
   P-ATA2 Cable Detection force    [Disabled]               | ESC    Exit
   Hard Disk Write Protect         [Disabled]               |
   IDE Detect Time Out (Sec)       [35]                     |
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```

Feature	Options	Description
IDE Configuration	Disable, **P-ATA Only**, S-ATA Only, P-ATA & S-ATA	Setup the configuration of the hard drive interfaces

When P-ATA & S-ATA mode is selected:

Feature	Options	Description
Combined Mode Option	**P-ATA 1st Channel**, S-ATA 1st Channel	Setup the configuration of the hard drive interfaces
S-ATA Ports Definition	**P0-Master/P1-Slave**, P0-Slave/P1-Master	Select physical ports (P0/P1) to be Master/Slave or Slave/Master

When S-ATA only mode is selected:

Feature	Options	Description
S-ATA Ports Definition	**P0-1st./P1-2nd.**, P0-2nd./P1-1st.	Select physical ports (P0/P1) to be 1st./2nd. or 2nd./1st.

When P-ATA only mode is selected:

Feature	Options	Description
S-ATA Running Enhanced Mode	**Yes**, No	Setup the S-ATA interface to be running in enhanced mode or legacy mode
P-ATA Channel Selection	Primary, Secondary, **Both**	Setup the active IDE channels
S-ATA Ports Definition	**P0-3rd./P1-4th**, P0-4th./P1-3rd	Select physical ports (P0/P1) to be 3rd/4th or 4th/3rd
Configure S-ATA as RAID	**No**, Yes	Only available when "P-ATA Only" is selected. Note: Install the driver via USB-Floppy connected to USB port 2 (lower conn.)

```
                         BIOS SETUP UTILITY
          Advanced
  Primary IDE Master                              Select the type of
                                                  devices connected to
  Device        :Hard Disk                        the system
  Vendor        :ST340014A
  Size          :40.0GB
  LBA Mode      :Supported
  Block Mode    :16Sectors
  PIO Mode      :4
  Async DMA     :MultiWord DMA-2
  Ultra DMA     :Ultra DMA-5
  S.M.A.R.T.    :Supported

  Type                            [Auto]          <-    Select Screen
  LBA/Large Mode                  [Auto]          ||    Select Item
  Block (Multi-Sector Transfer)   [Auto]          +-    Change Option
  PIO Mode                        [Auto]          F1    General Help
  DMA Mode                        [Auto]          F10   Save and Exit
  S.M.A.R.T.                      [Auto]          ESC   Exit
  32Bit Data Transfer             [Disabled]

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```

Feature	Options	Description
Type	Not Installed, **Auto,** CDROM, ARMD	Select the type of device installed
LBA/Large Mode	Disabled, **Auto**	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors.
Block (Multi-Sector Transfer)	Disabled, **Auto**	Select if the device should run in Block mode
PIO Mode	**Auto**, 0, 1, 2, 3, 4	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
DMA Mode	**Auto**, SWDMA0, SWDMA1, SWDMA2, MWDMA0, MWDMA1, MWDMA2, UDMA0, UDMA1, UDMA2, UDMA3, UDMA4, UDMA5	Selects the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. **Note: To use UDMA Mode 2, 3, 4 and 5 with a device, the harddisk cable used MUST be UDMA66/100 cable (80-conductor cable).**
S.M.A.R.T.	**Auto**, Disabled, Enabled	Select if the Device should be monitoring itself (Self-Monitoring, Analysis and Reporting Technology System)
32Bit Data Transfer	**Disabled**, Enabled	Select if the Device should be using 32Bit data Transfer

Feature	Options	Description
ATA(PI) 80Pin Cable Detection	**Host & Device**, Host, Device	Select the mechanism for detecting 80Pin ATA Cable
P-ATA1 Cable Detection Force	**Disable**, 40Pin, 80Pin	Force the board to operate as if a 40Pin ATA cable or 80Pin ATA cable is installed on the Primary channel
P-ATA2 Cable Detection Force	**Disable**, 40Pin, 80Pin	Force the board to operate as if a 40Pin ATA cable or 80Pin ATA cable is installed on the Primary channel
Hard Disk Write Protect	**Disable**, Enabled	Enable write protection on HDDs, only works when it is accessed through the BIOS
IDE Detect Time Out (Sec)	0, 5, 10, 15, 20, 25, 30, **35**	Select the time out value when the BIOS is detecting ATA/ATAPI Devices

8.3.3 Advanced settings – LAN Configuration

```
                         BIOS SETUP UTILITY
        Advanced
   LAN Configuration                                    Control of Ethernet
                                                        Devices and RPL/PXE
   ETH1 Configuration              [With RPL/PXE boot]  boot
     MAC Address                   : 00E0F4000001
   ETH2 Configuration              [Enabled]
     MAC Address                   : 00E0F4000002
   ETH3 Configuration              [Enabled]
     MAC Address                   : 00E0F4000003

                                                        <-     Select Screen
                                                        ||     Select Item
                                                        +-     change option
                                                        F1     General Help
                                                        F10    Save and Exit
                                                        ESC    Exit
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```

Feature	Options	Description
ETH1 Configuration	Disabled, **Enabled,** With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom
ETH2 Configuration	Disabled, **Enabled,** With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom
ETH3 Configuration	Disabled, **Enabled,** With RPL/PXE boot	Select if you want to enable the LAN adapter, or if you want to activate the RPL/PXE boot rom

8.3.4 Advanced settings – Floppy Configuration

```
                         BIOS SETUP UTILITY
            Advanced
 Floppy Configuration                          | Select the type of
                                               | floppy drive connected
 Floppy A                       [Disabled]     | to the system
 Floppy B                       [Disabled]     |
                                               |
                                               | <-    Select Screen
                                               | ||    Select Item
                                               | +-    change option
                                               | F1    General Help
                                               | F10   Save and Exit
                                               | ESC   Exit
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```

Feature	Options	Description
Floppy A	**Disabled,** 360KB, 1.2MB, 720KB, 1.44MB, 2.88MB	Select Floppy device installed in the system using the LPT->Floppy cable
Floppy B	**Disabled,** 360KB, 1.2MB, 720KB, 1.44MB, 2.88MB	Select Floppy device installed in the system using the LPT->Floppy cable

Notes: Enter SuperIO Configuration and enable Onboard Floppy Controller.
Parallel port can not be used if Onboard Floppy Controller is enabled.

8.3.5 Advanced settings – SuperIO Configuration

```
                         BIOS SETUP UTILITY
          Advanced
   Configure Win627THF Super IO Chipset              Enable onboard Floppy
                                                     Controller for use at
   OnBoard Floppy Controller      [Disabled]         parallel port
   Serial Port1 Address           [3F8/IRQ4]
   Serial Port2 Address           [2F8/IRQ3]
     Serial Port2 Mode            [Normal]
   Parallel Port Mode             [378]
     Parallel Port Mode           [Normal]           <-     Select Screen
     Parallel Port IRQ            [IRQ7]             ||     Select Item
   ICH SIO Serial Port1 Addresse  [Disabled]         +-     change option
   ICH SIO Serial Port2 Addresse  [Disabled]         F1     General Help
                                                     F10    Save and Exit
                                                     ESC    Exit

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```

Feature	Options	Description
OnBoard Floppy Controller	**Disabled**, Enabled	Enable or disable the Floppy Controller
Serial Port1 Address	Disabled, **3F8/IRQ4**, 3E8/IRQ4, 3E8/IRQ6, 3E8/IRQ10, 2E8/IRQ11	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).
Serial Port2 Address	Disabled, **2F8/IRQ3**, 2E8/IRQ3, 3E8/IRQ6, 3E8/IRQ10, 2E8/IRQ11	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).
Serial Port2 Mode	**Normal**, IRDA, ASK IR	Select Mode for Serial Port2
Parallel Port Address	Disabled, **378**, 278, 3BC	Select the I/O address for the LPT. **NOTE:** you cannot enable the floppy controller and parallel port at the same time!
Parallel Port Mode	**Normal**, Bi-Directional, EPP, ECP	Select the mode that the parallel port will operate in
EPP Version	1.9, 1.7	Setup with version of EPP you want to run on the parallel port
ECP Mode DMA Channel	DMA0, DMA1, DMA3	Select a DMA channel
Parallel Port IRQ	IRQ5, **IRQ7**	Select a IRQ
ICH SIO Serial Port1 Address	**Disabled**, 3E8/IRQ6, 3E8/IRQ10, 2E8/IRQ11	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).
ICH SIO Serial Port2 Address	**Disabled**, 3E8/IRQ6, 3E8/IRQ10, 2E8/IRQ11	Select the BASE I/O addresse and IRQ. (The available options depends on the setup for the the other Serial Ports).

8.3.6 Advanced settings – Hardware Health Configuration

```
                           BIOS SETUP UTILITY
              Advanced
   Hardware Health Event Monitoring                       Disable = Full Speed

   System Temperature            :37ºC/98ºF               Thermal: Does regulate
   CPU Temperature               :43ºC/109ºF              fan speed according to
   External Temperature Sensor   :N/A                     specified temperature

   Fan1 Speed                    :Fail                    Speed: Does regulate
     Fan Cruise Control             [Disabled]            according to specified
   Fan2 Speed                    :2537 RPM                RTM
     Fan Cruise Control             [Thermal]
     Fan Setting                    [45°C/113°F]
   Fan3 Speed                    :2164
     Fan Cruise Control             [Speed]
     Fan Setting                    [2177 RPM]

   Watchdog Function                [Disabled]

                                                          <-     Select Screen
                                                          ||     Select Item
                                                          +-     change option
                                                          F1     General Help
                                                          F10    Save and Exit
                                                          ESC    Exit
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```

Feature	Options	Description
Fan Cruise Control	**Disabled**, Thermal, Speed	Select how the Fan shall operate. When set to Thermal, the Fan will start to run at the CPU die temperature set below. When set to Speed, the Fan will run at the Fixed speed set below.
Fan Settings	1406-5625 RPM, 30°-75°C	The fan can operate in Thermal mode or in a fixed fan speed mode

Feature	Options	Description
Watchdog	**Disabled**, 16 seconds, 38 seconds, 1 minute, 2 minutes, 5 minutes, 10 minutes	Adjust the amounts of boot time allowed before system reset occurs. Software must disable or reload timer. Disable, IO 869h BIT3 Init value 861h = 4-3Fh = 2.4 – 38 sec Reload, write to 860h

8.3.7 Advanced settings – Voltage Monitor

```
                         BIOS SETUP UTILITY
         Advanced
   Voltage Monitor                                  Enable Hardware Health
                                                    Monitoring Device.
   Requested Core                :1.484 V
   VcoreA                        :1.431 V

   VcoreB                        :1.483 V
   +3.3Vin                       :3.290 V
   +5Vin                         :4.985 V
   +12Vin                        :12.016 V
   -12Vin                        :Good
   +5VSB                         :5.012 V
                                                    <-    Select Screen
                                                    ||    Select Item
                                                    +-    change option
                                                    F1    General Help
                                                    F10   Save and Exit
                                                    ESC   Exit
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```

8.3.8 Advanced settings – ACPI Configuration

```
                         BIOS SETUP UTILITY
         Advanced
   ACPI Settings                                    Enable Hardware Health
                                                    Monitoring Device.
   ACPI Aware O/S                 [Yes]

>  General ACPI Configuration
>  Advanced ACPI Configuration

                                                    <-    Select Screen
                                                    ||    Select Item
                                                    +-    change option
                                                    F1    General Help
                                                    F10   Save and Exit
                                                    ESC   Exit
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```

Feature	Options	Description
ACPI Aware O/S	**Yes**, No	Select if your O/S supports ACPI

8.3.9 Advanced settings – General ACPI Configuration

```
                         BIOS SETUP UTILITY
            Advanced
   General ACPI Configuration                        | Select the ACPI state
                                                     | used for System
   Suspend mode                  [S1 & S3 (STR)]     | Suspend.
   Repost Video on S3 Resume     [No]                |
   S4BIOS Support                [Disabled]          |
                                                     |
                                                     | <-     Select Screen
                                                     | ||     Select Item
                                                     | +-     change option
                                                     | F1     General Help
                                                     | F10    Save and Exit
                                                     | ESC    Exit
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```

Feature	Options	Description
Suspend mode	S1 (POS) only, **S1&S3 (STR)**	Select the ACPI state used for System Suspend
Repost Video on S3 Resume	**No**, Yes	Determines whether to invoke VGA BIOS post on S3/STR resume
S4BIOS Support	**Disabled**, Enabled	Determines if you want to support S4 power state

8.3.10 Advanced settings – Advanced ACPI Configuration

```
                          BIOS SETUP UTILITY
         Advanced
   Advanced ACPI Configuration                            | Enable RSDP pointers
                                                          | to 64-bit Fixed System
   ACPI 2.0 Features              [No]                    | Description Tables.
   ACPI APIC support              [Enabled]               |
   APIC ACPI SCI IRQ              [Disabled]              |
   AMI OEMB table                 [Enabled]               |
   Headless mode                  [Disabled]              |
                                                          | <-     Select Screen
                                                          | ||     Select Item
                                                          | +-     change option
                                                          | F1     General Help
                                                          | F10    Save and Exit
                                                          | ESC    Exit
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```

Feature	Options	Description
ACPI 2.0 Features	**No**, Yes	Enable/ Disable ACPI 2.0 features
ACPI APIC support	**Enabled**, Disabled	Setup if the APIC controller should be supported in the ACPI code
APIC ACPI SCI IRQ	Enabled, **Disabled**	Enable/ Disable APIC ACPI SCI IRQ
AMI OEMB table	**Enabled**, Disabled	Enable/ Disable AMI OEMB table
Headless mode	Enabled, **Disabled**	Enable/ Disable Headless mode

8.3.11 Advanced settings – Remote Access Configuration

```
                         BIOS SETUP UTILITY
        Advanced
   Configure Remote Access type and parameters      | Enable RSDP pointers
                                                    | to 64-bit Fixed System
   Remote Access                  [Enabled]         | Description Tables.
                                                    |
   Serial port number             [ICH COM1]        |
   Serial Port Mode               [115200 8,n,1]    |
   Flow Control                   [None]            |
   Redirection After BIOS POST    [Always]          |
                                                    |
   Terminal Type                  [ANSI]            |
   VT-UTF8 Combo Key Support      [Disabled]        | <-     Select Screen
                                                    | ||     Select Item
                                                    | +-     change option
                                                    | F1     General Help
                                                    | F10    Save and Exit
                                                    | ESC    Exit
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```

Feature	Options	Description
Remote Access (Settings below not displayed if Remote Access is disabled)	**Disabled**, Enabled	Allows you to see the screen over the comport interface, in a terminal window
Serial port number	SIO COMA **SIO COMB**	Setup which comport that should be used for communication
Serial Port Mode	**115200 8 n 1** 57600 8 n 1 38400 8 n 1 19200 8 n 1 9600 8 n 1	Select the serial port speed
Flow Control	**None** Hardware Software	Select Flow Control for serial port
Redirection After BIOS POST	Disabled Boot Loader **Always**	How long shall the BIOS send the picture over the serial port
Terminal Type	**ANSI** VT100 VT-UTF8	Select the target terminal type
VT-UTF8 Combo Key Support	**Disabled** Enabled	Setup VT-UTF8 Combo Key

8.3.12 Advanced settings – USB Configuration

```
                         BIOS SETUP UTILITY
          Advanced
   USB Configuration                                  | Enables USB host
                                                      | controllers.
   Module Version – 2.24.0-11.4                       |
                                                      |
   USB Devices Enabled :                              |
     1 Drive                                          |
                                                      |
   USB Function                  [All USB Ports]      |
   Legacy USB Support            [Enabled]            |
   USB 2.0 Controller            [Enabled]            |
   USB 2.0 Controller Mode       [HiSpeed]            |
                                                      |
 > USB Mass Storage Device Configuration              | <-     Select Screen
                                                      | ||     Select Item
                                                      | +-     change option
                                                      | F1     General Help
                                                      | F10    Save and Exit
                                                      | ESC    Exit
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```

Feature	Options	Description
USB Function	Disabled, 2 USB Ports, **All USB Ports**	Select the USB ports you want to enabled
Legacy USB Support	Disabled, **Enabled**, Auto	Support for legacy USB Keyboard
USB 2.0 Controller	**Enabled**, Disabled	Setup the USB 2 controller (480Mbps)
USB 2.0 Controller Mode (only if USB Controller = Enabled)	FullSpeed, **HiSpeed**	Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps)
BIOS EHCI Hand-Off	**Enabled**, Disabled	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI Driver.

8.3.13 Advanced settings – USB Mass Storage Device Configuration

```
                     BIOS SETUP UTILITY
        Advanced
  USB Mass Storage Device Configuration          Enables USB host
                                                 controllers.
  USB Mass Storage Reset Delay   [20 Sec]

     Device #1                   JetFlash TS256MJF2L
     Emulation Type              [Auto]

                                                 <-     Select Screen
                                                 ||     Select Item
                                                 +-     change option
                                                 F1     General Help
                                                 F10    Save and Exit
                                                 ESC    Exit
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```

Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec, **20 Sec**, 30 Sec, 40 Sec	Number of seconds the BIOS waits for the USB device after start unit command
Emulation Type	**Auto**, Floppy, Forced FDD, Hard Disk, CDROM	Setup the emulation type for the USB device

8.4 PCIPnP Menu

```
                         BIOS SETUP UTILITY
                    PCIPnP
   Advanced PCI/PnP Settings                              NO: lets the BIOS
                                                          configure all the
   Warning: Setting wrong values in below sections       devices in the system.
            May cause system to malfunction.              YES: lets the
                                                          operating system
   Plug & Play O/S                [No]                    configure Plug and
   PCI Latency Timer              [64]                    Play (PnP) devices not
   Allocate IRQ to PCI VGA        [Yes]                   required for boot if
   PCI IDE BusMaster              [Enabled]               your system has a Plug
   IRQ5                           [Available]             and Play operating
   IRQ7                           [Available]             system.
   PCI Riser Support              [Disabled]
   Disable Unsed PCI Clocks       [Auto]                  <-    Select Screen
   Spread Spectrum Mode           [Disabled]              ||    Select Item
                                                          +-    change option
   PCI Slot-1 IRQ Preference      [Auto]                  F1    General Help
                                                          F10   Save and Exit
                                                          ESC   Exit
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```

Feature	Options	Description
Plug & Play O/S	**No,** Yes	Select if you have a PnP O/S
PCI Latency Timer	32, **64**, 96, 128, 160, 192, 224, 248	Value in units of PCI clocks for PCI device latency timer register
Allocate IRQ to PCI VGA	**Yes**, No	Assigns IRQ to PCI VGA card
PCI IDE BusMaster	**Enabled**, Disabled	Setup PCI bus mastering for read/write to IDE drives
IRQ5	**Available** Reserved	Available: can be used for PCI/PnP Reserved: can be used for legacy ISA
IRQ7	**Available** Reserved	Available: can be used for PCI/PnP Reserved: can be used for legacy ISA
PCI Riser Support	**Disabled**, PCI Slot3, PCI Slot2, PCI Slot1	Disabled as default and also when using the Kontron 820982 Riser card. Setup if using a PCI Riser card as described in section “886LCD-M PCI IRQ & INT routing”.
Disable Unused PCI Clocks	**Auto**, No	Disables PCI clocks if no PCI card is detected
Spread Spectrum	**Disabled**, Enabled	A technique for spreading the signal bandwidth over a wide range of frequencies to lower Radiated Emission
PCI Slot-1 IRQ Preference	**Auto** 5, 6, 7, 9, 10, 11	Manual IRQ selection does not guarantee PCI slot device will be configured with choice. WARNING: Selected IRQ will not be allowed for other devices.

8.5 Boot Menu

```
                          BIOS SETUP UTILITY
    Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
   Boot Settings                                   | Configure Settings
                                                   | during System Boot.
 > Boot Settings Configuration                     |
                                                   |
 > Boot Device Priority                            |
                                                   | <-    Select Screen
   Auto adjust Boot Priority      [Yes]            | ||    Select Item
   Removable Devices 1st          [No]             | Enter Go to Sub Screen
   Force Boot Device              [Disabled]       | F1    General Help
   F11 BBS popup boot menu        [Enabled]        | F10   Save and Exit
     Hide Removable Devices       [No]             | ESC   Exit
   Execute Embedded Firmware      [Disabled]       |
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```

8.5.1 Boot – Boot Settings Configuration

```
                          BIOS SETUP UTILITY
                                 Boot
   Boot Settings                                   | Configure Settings
                                                   | during System Boot.
   Quick Boot                        [Enabled]     |
   Quiet Boot                        [Disabled]    |
   Bootup Num-Lock                   [On]          | <-    Select Screen
   PS/2 Mouse Support                [Auto]        | ||    Select Item
   Halt on                           [All, But Keyboard] | Enter Go to Sub Screen
   Hit 'DEL' Message Display         [Enabled]     | F1    General Help
   Interrupt 19 Capture              [Disabled]    | F10   Save and Exit
                                                   | ESC   Exit
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```

Feature	Options	Description
Quick Boot	**Enabled** Disabled	Allows BIOS to skip certain test while booting
Quiet Boot	**Disabled** Enabled Enabled & Maintain	Shows boot logo instead of POST screen
Bootup Num-Lock	Off, **On**	Select Power-on state for numlock
PS/2 Mouse Support	Disabled Enabled **Auto**	Select support for PS/2 Mouse
Halt on (see note)	Disabled **All But Keyboard**	Wait for F1 key to be pressed if error. If no keyboard present post will continue
Hit 'DEL' Message Display	Disabled **Enabled**	Display the message or not
Interrupt 19 Capture	**Disabled** Enabled	Allows option ROMs to trap interrupt 19

Note: List of errors:

<INS> Pressed
Timer Error
Interrupt Controller-1 error
Keyboard/Interface Error
Halt on Invalid Time/Date
NVRAM Bad
Primary Master Hard Disk Error
S.M.A.R.T HDD Error
Cache Memory Error
DMA Controller Error
Resource Conflict
Static Resource Conflict
PCI I/O conflict
PCI ROM conflict
PCI IRQ conflict
PCI IRQ routing table error

Feature	Options	Description
Auto adjust Boot Priority	**Yes** No	If Yes then eg. USB devices will be placed first in the boot Device Priority Menu when booting.
Removable Devices 1st	**No** Yes	Should removable USB devices get first boot priority when inserted
Force Boot Device	**Disabled** Primary IDE Master Primary IDE Slave Secondary IDE Master Secondary IDE Slave Third IDE Master Forth IDE Master Any Harddrive (above) Network	Does overwrite current boot setting. Device must be in the boot priority menu though. If the device fails to boot, the system will not try other devices.
F11 BBS popup boot menu	Disabled **Enabled** Full Access	Disabled: hide F11 BBS post setup message. Enabled: F11 post unless Force Boot Device. Full Access: F11 post
Hide Removable Devices	**No** Yes	Hide Removable Devices in BBS POPUP menu (F11)
Execute Embedded Firmware	**Disabled** Enabled	Execute OEM software if embedded into BIOS. (Default MemTest-86)

8.6 Security Menu

```
                          BIOS SETUP UTILITY
   Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
   Security Settings                                   Install or Change the
                                                       password.
   Supervisor Password :Installed
   User Password       :Installed

   Change Supervisor Password
   Change User Password
   Clear User Password

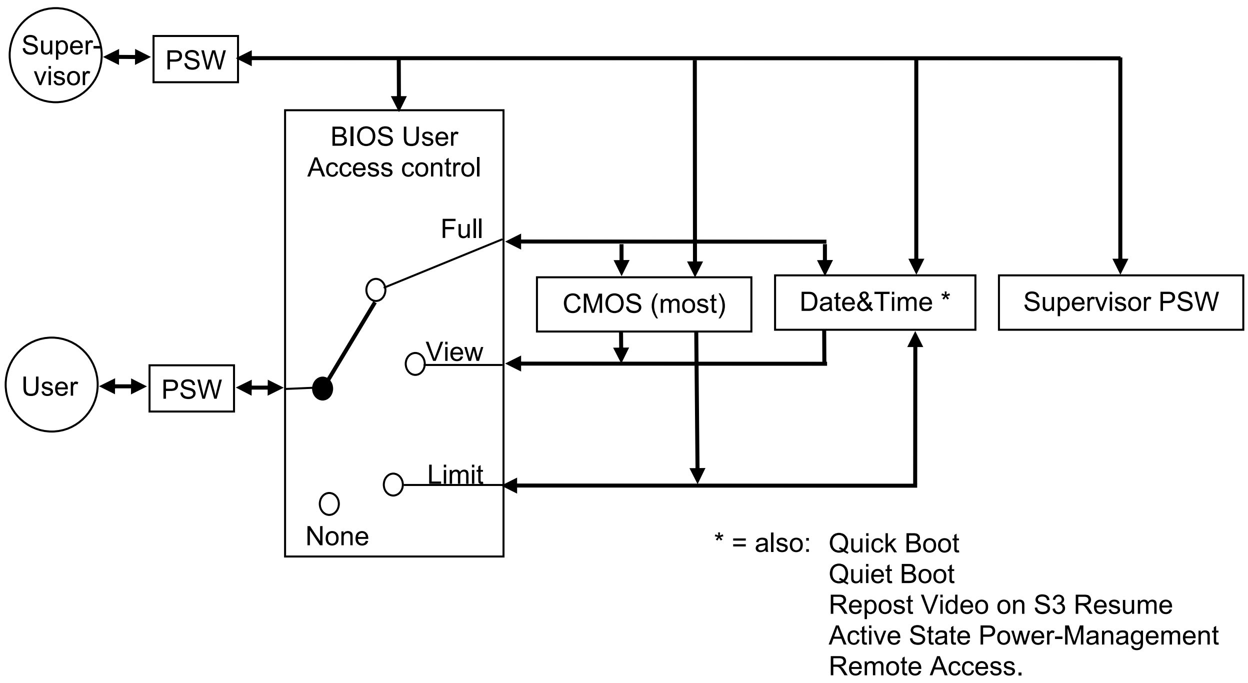
   Boot Sector Virus Protection    [Disabled]

   Hard Disk Security                                  <-    Select Screen
   ------------------------------------------------------  ||    Select Item
   Primary Master HDD User Password                    Enter Go to Sub Screen
   Primary Slave HDD User Password                     F1    General Help
   Secondary Slave HDD User Password                   F10   Save and Exit
                                                       ESC   Exit

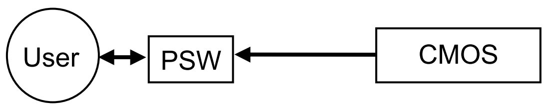
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```

Feature	Options	Description
Change Supervisor Password	Password	When not cleared the advanced Supervisor Password protection system is enabled (see below diagram). Hereafter setting can only be accessed when entering BIOS as Supervisor.
User Access Level	**Full Access** View Only Limited No Access	Only visible if Supervisor Password is installed. Full Access: User can change all BIOS settings. View Only: User can only read BIOS settings. Limited: User can only read settings except: Date & Time, Quick Boot, Quiet Boot, Repost Video on S3 Resume, Active State Power-Management and Remote Access. No Access: User can not enter BIOS, but if Password Check = Always then User password will allow boot.
Change User Password	Password	Change the User Password
Clear User Password	Ok Cancel	Clears the User Password
Boot Sector Virus Protection	Enabled **Disabled**	Will write protect the MBR when the BIOS is used to access the harddrive
HDD Password	Password	Locks the HDD with a password, the user needs to type the password on power on

Supervisor Password protection (setup Supervisor before User)



User Password protection only (no Supervisor Password used)



8.7 Chipset Menu

```
                         BIOS SETUP UTILITY
   Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
   Advanced Chipset Settings                            Intel Montara-GML
                                                        NorthBridge chipset
   Warning: Setting wrong values in below sections      configuration options.
            may cause system to malfunction.

>  Intel Montara-GML NorthBridge Configuration
>  SouthBridge Configuration

   Boot Type:                        [CRT+LFP]
   Backlight Signal Inversion        [Disabled]
   LCDVCC Voltage                    [5V]               <-    Select Screen
   Backlight PWM modulation          [10KHz]            ||    Select Item
   Backlight PWM ratio               [50%]              Enter Go to Sub Screen
                                                        F1    General Help
   EDID Support                      [Enabled]          F10   Save and Exit
   LVDS                              [LM201U03]         ESC   Exit
   DVO                               [N/A]
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```

8.7.1 Advanced Chipset Settings – Intel Montara-GML NorthBridge Configuration

```
                         BIOS SETUP UTILITY
                                                     Chipset
   Configure advanced settings for NorthBrigde          Select which graphics
                                                        controller to use as
   Primary Video Device             [Auto]              the primary boot
   Graphics Mode Select             [Enabled, 8MB]      device.
   IGD – Device 2,Function 1:       [Enabled]

                                                        <-    Select Screen
                                                        ||    Select Item
                                                        Enter Go to Sub Screen
                                                        F1    General Help
                                                        F10   Save and Exit
                                                        ESC   Exit
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```

Feature	Options	Description
Primary Video Device	Internal External PCI External AGP **Auto**	Select which graphics controller to use as the primary boot device
Graphics Mode Select	Disabled, 1MB, 4MB, **8MB**, 16MB, 32MB	Select the amount of system memory used by the internal graphics device
IGD – Device 2, Function 1	Disabled **Enabled**	Setup the multimonitor function

8.7.2 Advanced Chipset Settings – SouthBridge Configuration

```
                         BIOS SETUP UTILITY
                                                 Chipset
                                               | Enable / Disable the
                                               | ICH4 IOAPIC function.
   IOAPIC                        [Enabled]     |
   Extended IOAPIC               [Enabled]     | <-    Select Screen
   OnBoard AC'97 Audio           [Enabled]     | ||    Select Item
   OnBoard Amplifier             [Enabled]     | Enter Go to Sub Screen
                                               | F1    General Help
                                               | F10   Save and Exit
                                               | ESC   Exit
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```

Feature	Options	Description
IOAPIC	Disabled **Enabled**	Setup the ICHS IOAPIC function
Extended IOAPIC	Disabled **Enabled**	Setup the extended mode of ICHS IOAPIC
OnBoard AC'97 Audio	Disabled **Enabled**	Setup the onboard audio
OnBoard Amplifier	Disabled **Enabled** Enabled Early	If Enabled the AMP is turned on after boot. If Early, bios beeps will be out as "PC Beep" is routed through codec. Problems with DRAM will be announced through AMP regardless of this setting.

Feature	Options	Description
Boot Type	VBIOS Default **CRT** LFP CRT+LFP EFP TV CRT+EFP CRT+TV EFP+EFP2 EFP+TV	Setup type of boot screen
Backlight Signal Inversion	Disabled **Enabled**	Select the signal polarity
LCDVCC Voltage	**3.3V** 5V	Setup the LCD Voltage
Backlight PWM modulation	1KHz 5KHz **10KHz** 20KHz	Backlight intensity PWM signal frequency setup
Backlight PWM ratio	0%, 12.5%, 25% 37.5%, **50%,** 62.5% 75%, 87.5%, 100%	Backlight intensity PWM signal pulse width setup
EDID Support	**Enabled** Disabled	LVDS auto configuration via EEProm
LVDS	Panels	Chose the connected LVDS panel
DVO	DVO Chip	Select the DVO connection

8.8 Power Menu

```
                              BIOS SETUP UTILITY
   Main     Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
                                                       | Enable/Disable SMI
  ADVANCED SMI ENABLE CONTROLS                         | based power management
  Power Management/APM          [Enabled]              | and APM support.
  Power Button Mode             [On/Off]               |
                                                       |
  ADVANCED RESUME EVENT CONTROLS                       |
  USB Controller Resume         [Disabled]             |
  PME Resume                    [Disabled]             |
  RI Resume                     [Disabled]             |
                                                       |
  RTC Resume                    [Enabled]              |
    RTC Alarm Data              [11]                   |
    RTC Alarm Time              [11:11:11]             |
                                                       | <-     Select Screen
                                                       | ||     Select Item
  PS/2 Kbd/Mouse S4/S5 Wake     [Disabled]             | +-     Change Option
  S3-S5 Keyboard Hotkey         [Any key]              | F1     General Help
                                                       | F10    Save and Exit
  AC Power Loss Restart         [Off]                  | ESC    Exit

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```

Feature	Options	Description
Power Management/APM	Disabled **Enabled**	Setup the SMI/APM support
Power Button Mode	**On/Off** Suspend	Select Power button functionality
USB Controller Resume	Disabled **Enabled**	Lets the USB devices wake up from sleep state
PME/WOL	**Disabled** Enabled	Allow PME/WOL to wake from sleep states
RI Resume	**Disabled** Enabled	Allow RI/Modem to wake from sleep states
RTC Resume	Enabled **Disabled**	Let the board start up on a specific date and time
RTC Alarm Date	Every Day 1-31	Setup the date you want the board to start
RTC Alarm Time	HH:MM:SS	Setup the time you want the board to start
PS/2 Kbd/Mouse S4/S5 Wake	**Disabled** Enabled	When disabled the board can wake from S1 and S3, and when enabled it can also wake from S4 and S5
S3-S5 Keyboard Hotkey	**Any key** Space Enter Sleep button	Setup the key that can wake up the board
AC Power Loss Restart	**Off** On Previous State	Select whether or not to restart the system after AC power loss: **Off** keeps the power off until the power button is pressed. **On** restores power to the computer. **Previous State** restores the previous power state before power loss occurred.

8.9 Exit Menu

```
                          BIOS SETUP UTILITY
  Main    Advanced    PCIPnP    Boot    Security    Chipset    Power    Exit
   Exit Options                                        | Exit system setup
                                                       | after saving the
   Save Changes and Exit                               | changes.
   Discard Changes and Exit                            |
   Discard Changes                                     | F10 Key can be used
                                                       | for this operation.
   Load Optimal Defaults                               |
   Load Failsafe Defaults                              |
  ______________________________________________________|
                                                       |
   Halt on invalid Time/Date       [Enabled]           |
   Secure CMOS                     [Disabled]          |
                                                       |
                                                       | <-     Select Screen
                                                       | ||     Select Item
                                                       | Enter  Go to Sub Screen
                                                       | F1     General Help
                                                       | F10    Save and Exit
                                                       | ESC    Exit
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```

Feature	Options	Description
Save Changes and Exit	Ok Cancel	Exit system setup after saving the changes
Discard Changes and Exit	Ok Cancel	Exit system setup without saving any changes
Discard Changes	Ok Cancel	Discards changes done so far to any of the setup questions
Load Optimal Defaults	Ok Cancel	Load Optimal Default values for all the setup questions
Load Failsafe Defaults	Ok Cancel	Load Failsafe Default values for all the setup questions
Halt on invalid Time/Date	**Enabled** Disabled	Shall the BIOS halt and wait for a keypress when the cmos is corrupted
Secure CMOS	**Disabled** Enabled	Enable will store the current CMOS in the BIOS flash rom, this will maintain the settings even if the battery is failing

8.10 AMI BIOS Beep Codes

Boot Block Beep Codes:

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

POST BIOS Beep Codes:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

Troubleshooting POST BIOS Beep Codes:

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

9. OS setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on the 886LCD-M Driver CD or they can be downloaded from the homepage www.kontron-emea.com

Note: When installing/using ADD cards like ADD-DVI or ADD-LVDS it's possible that the OS start up without any connected display(s) active. If you are able to pass the "Log On to Windows" etc. by entering the password etc. without actually see the picture on the display and If the Hot Keys have not been disabled in the Extreme Graphic driver then the following key combinations you can select a connected display:

<Ctrl><Alt><F1> enables the CRT (on board)
<Ctrl><Alt><F3> enables the LVDS (on board)
<Ctrl><Alt><F4> enables display conneted to the ADD card.

10. Warranty

KONTRON Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period, KONTRON Technology will, at its sole option, repair or replace the product with a similar product. Replacement Product or parts may include remanufactured or refurbished parts or components.

The warranty does not cover:

1. Damage, deterioration or malfunction resulting from:
   A. Accident, misuse, neglect, fire, water, lightning, or other acts of nature, unauthorized product modification, or failure to follow instructions supplied with the product.
   B. Repair or attempted repair by anyone not authorized by KONTRON Technology.
   C. Causes external to the product, such as electric power fluctuations or failure.
   D. Normal wear and tear.
   E. Any other causes which does not relate to a product defect.
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2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.